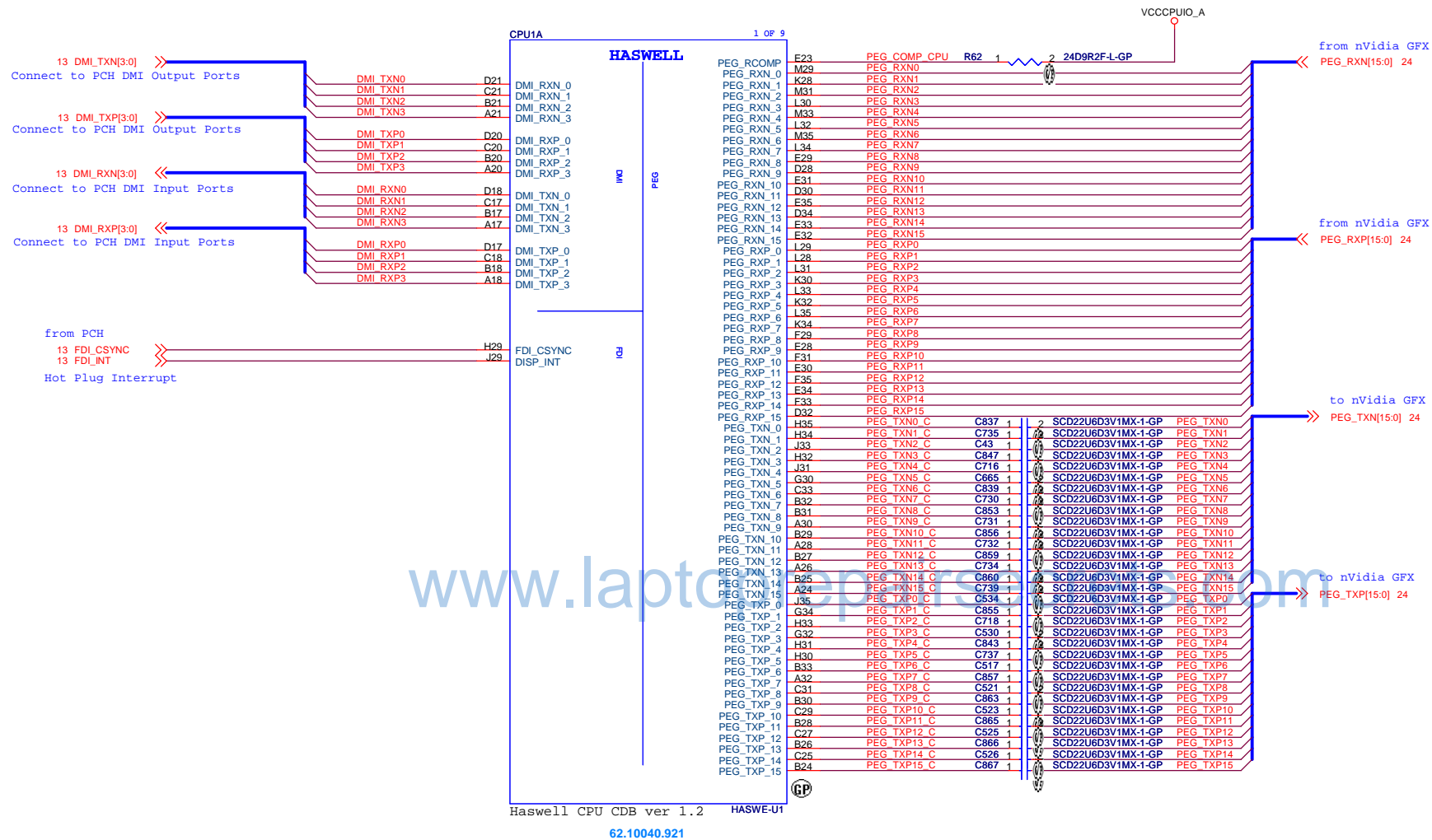


Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 >=> 1/16W, 75V 0805 >=> 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

Symbol name	Value	Tolerance (B: +/-0.1p, C: +/-0.25p, D: +/-0.5p) (K: +/-10%, M: +/-20%, Z: +80/-20%)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

PCH GPIO <sub>n</sub>	39	38	49	48	Planar ID Version	Planar PCB Version
PLANAR_ID <sub>n</sub>	3	2	1	0		
	0	0	0	0	SDV on 1/18	SA
	0	0	1	0	ME-FVT on 3/14	SB
	0	0	1	1	FVT on 4/11	SC
	0	0	1	1	ME-SIT on 5/24	SC
	0	1	0	0	SIT on 6/10	SD
	0	1	0	1	SIT-R on 7/22	SE
	0	1	1	0	SVT on 8/12	-1

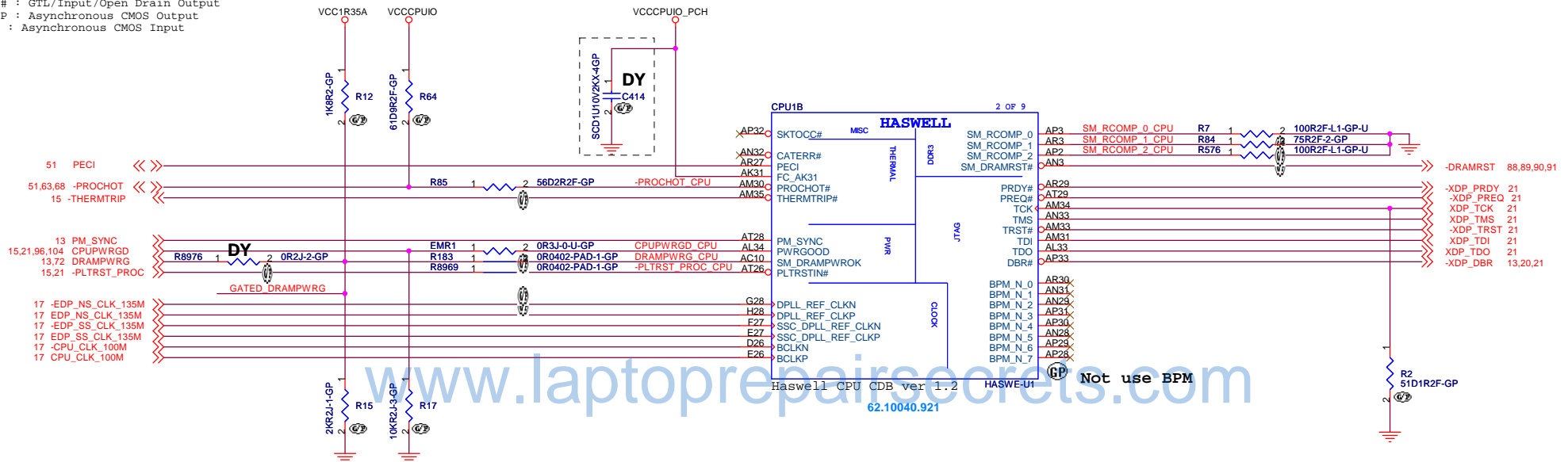
[illegible]



PEG Configuration  
Port 15 - 0 ( Function 0 ) : x16 GFX

This Project does not have dual layout function to support next platform, So THERMTRIP# signal does not need to have external pullup as NO ASM.

PECI : Asynchronous Bidirectional  
 PROCHOT# : GTL/Input/Open Drain Output  
 THERMTRIP : Asynchronous CMOS Output  
 PM\_SYNC : Asynchronous CMOS Input



PECI has internal Pull Up to VCCIO\_OUT with 15~45ohm.

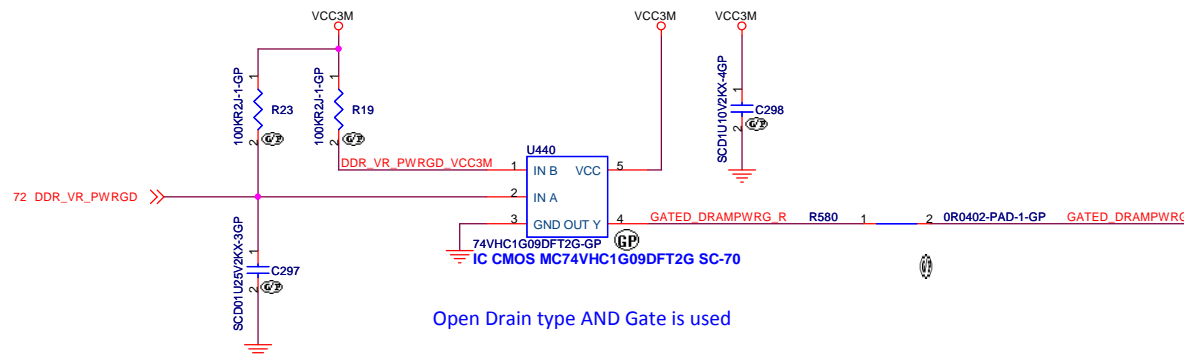
If Catastrophic Error (CATERR#) function is not required, This pin is left.

If Socket Occupied (SKTOCC#) function is not required, this pin is left.

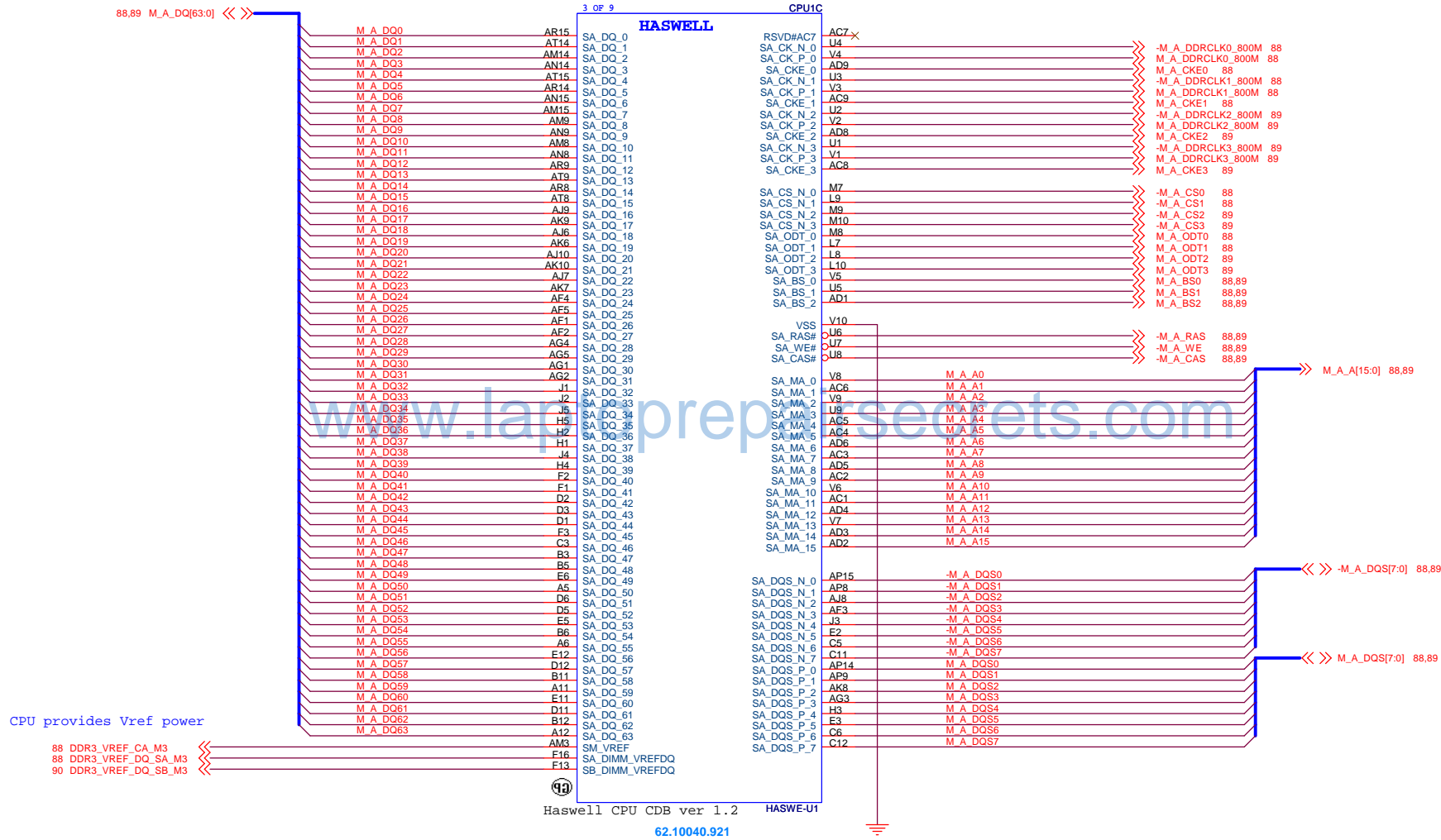
TMS and TDI has internal Pull Up to VCCIO\_TERM with 30~70ohm.

PREQ# has internal Pull Up to VCCIO\_OUT with 40~60ohm.

BPM[7:0] has internal Pull UP to VCCIO\_OUT with 40~60ohm.



Open Drain type AND Gate is used



90,91 M\_B\_DQ[63:0] << >>

M\_B\_DQ0  
M\_B\_DQ1  
M\_B\_DQ2  
M\_B\_DQ3  
M\_B\_DQ4  
M\_B\_DQ5  
M\_B\_DQ6  
M\_B\_DQ7  
M\_B\_DQ8  
M\_B\_DQ9  
M\_B\_DQ10  
M\_B\_DQ11  
M\_B\_DQ12  
M\_B\_DQ13  
M\_B\_DQ14  
M\_B\_DQ15  
M\_B\_DQ16  
M\_B\_DQ17  
M\_B\_DQ18  
M\_B\_DQ19  
M\_B\_DQ20  
M\_B\_DQ21  
M\_B\_DQ22  
M\_B\_DQ23  
M\_B\_DQ24  
M\_B\_DQ25  
M\_B\_DQ26  
M\_B\_DQ27  
M\_B\_DQ28  
M\_B\_DQ29  
M\_B\_DQ30  
M\_B\_DQ31  
M\_B\_DQ32  
M\_B\_DQ33  
M\_B\_DQ34  
M\_B\_DQ35  
M\_B\_DQ36  
M\_B\_DQ37  
M\_B\_DQ38  
M\_B\_DQ39  
M\_B\_DQ40  
M\_B\_DQ41  
M\_B\_DQ42  
M\_B\_DQ43  
M\_B\_DQ44  
M\_B\_DQ45  
M\_B\_DQ46  
M\_B\_DQ47  
M\_B\_DQ48  
M\_B\_DQ49  
M\_B\_DQ50  
M\_B\_DQ51  
M\_B\_DQ52  
M\_B\_DQ53  
M\_B\_DQ54  
M\_B\_DQ55  
M\_B\_DQ56  
M\_B\_DQ57  
M\_B\_DQ58  
M\_B\_DQ59  
M\_B\_DQ60  
M\_B\_DQ61  
M\_B\_DQ62  
M\_B\_DQ63

AR18  
AT18  
AM17  
AM18  
AR17  
AT17  
AN17  
AN18  
AT12  
AR12  
AN12  
AM11  
AT11  
AR11  
AM12  
AN11  
AR5  
AR6  
AM5  
AM6  
AT5  
AT6  
AN5  
AN6  
AJ4  
AK4  
AJ1  
AJ2  
AM1  
AN1  
AK2  
AK1  
L2  
M2  
L4  
M4  
L1  
M1  
L5  
M5  
G7  
J8  
G8  
G9  
J7  
J8  
G10  
J10  
A8  
B8  
A9  
B9  
D8  
E8  
D9  
E9  
F15  
D15  
A15  
B15  
E14  
D14  
A14  
B14

## HASWELL

SB\_DQ\_0  
SB\_DQ\_1  
SB\_DQ\_2  
SB\_DQ\_3  
SB\_DQ\_4  
SB\_DQ\_5  
SB\_DQ\_6  
SB\_DQ\_7  
SB\_DQ\_8  
SB\_DQ\_9  
SB\_DQ\_10  
SB\_DQ\_11  
SB\_DQ\_12  
SB\_DQ\_13  
SB\_DQ\_14  
SB\_DQ\_15  
SB\_DQ\_16  
SB\_DQ\_17  
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SB\_DQ\_52  
SB\_DQ\_53  
SB\_DQ\_54  
SB\_DQ\_55  
SB\_DQ\_56  
SB\_DQ\_57  
SB\_DQ\_58  
SB\_DQ\_59  
SB\_DQ\_60  
SB\_DQ\_61  
SB\_DQ\_62  
SB\_DQ\_63

CPU1D

RSVD#AG8  
SB\_CKN0  
SB\_CK0  
SB\_CKE\_0  
SB\_CKN1  
SB\_CK1  
SB\_CKE\_1  
SB\_CKN2  
SB\_CK2  
SB\_CKE\_2  
SB\_CKN3  
SB\_CK3  
SB\_CKE\_3  
SB\_CS\_N\_0  
SB\_CS\_N\_1  
SB\_CS\_N\_2  
SB\_CS\_N\_3  
SB\_ODT\_0  
SB\_ODT\_1  
SB\_ODT\_2  
SB\_ODT\_3  
SB\_BS\_0  
SB\_BS\_1  
SB\_BS\_2  
VSS  
SB\_RAS#  
SB\_WE#  
SB\_CAS#  
SB\_MA\_0  
SB\_MA\_1  
SB\_MA\_2  
SB\_MA\_3  
SB\_MA\_4  
SB\_MA\_5  
SB\_MA\_6  
SB\_MA\_7  
SB\_MA\_8  
SB\_MA\_9  
SB\_MA\_10  
SB\_MA\_11  
SB\_MA\_12  
SB\_MA\_13  
SB\_MA\_14  
SB\_MA\_15  
SB\_DQS\_N\_0  
SB\_DQS\_N\_1  
SB\_DQS\_N\_2  
SB\_DQS\_N\_3  
SB\_DQS\_N\_4  
SB\_DQS\_N\_5  
SB\_DQS\_N\_6  
SB\_DQS\_N\_7  
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SB\_DQS\_P\_2  
SB\_DQS\_P\_3  
SB\_DQS\_P\_4  
SB\_DQS\_P\_5  
SB\_DQS\_P\_6  
SB\_DQS\_P\_7

AG8  
Y4  
AA4  
AF10  
Y3  
AA3  
AG10  
Y2  
AA2  
AG9  
Y1  
AA1  
AF9  
P4  
R2  
P3  
P1  
R4  
R3  
R1  
P2  
R7  
P6  
AA9  
R10  
R6  
P6  
P7  
R8  
Y5  
Y10  
AA5  
Y7  
AA6  
Y6  
AA7  
Y8  
AA10  
R9  
Y9  
AF7  
P9  
AA8  
AG7  
AP18  
AP11  
AP5  
AJ3  
L3  
H9  
C4  
C14  
AP17  
AP12  
AP6  
AK3  
M3  
H8  
C9  
C15

-M\_B\_DDRCLK0\_800M 90  
M\_B\_DDRCLK0\_800M 90  
M\_B\_CKE0 90  
-M\_B\_DDRCLK1\_800M 90  
M\_B\_DDRCLK1\_800M 90  
M\_B\_CKE1 90  
-M\_B\_DDRCLK2\_800M 91  
M\_B\_DDRCLK2\_800M 91  
M\_B\_CKE2 91  
-M\_B\_DDRCLK3\_800M 91  
M\_B\_DDRCLK3\_800M 91  
M\_B\_CKE3 91  
-M\_B\_CS0 90  
-M\_B\_CS1 90  
-M\_B\_CS2 91  
-M\_B\_CS3 91  
M\_B\_ODT0 90  
M\_B\_ODT1 90  
M\_B\_ODT2 91  
M\_B\_ODT3 91  
M\_B\_BS0 90,91  
M\_B\_BS1 90,91  
M\_B\_BS2 90,91  
-M\_B\_RAS 90,91  
-M\_B\_WE 90,91  
-M\_B\_CAS 90,91  
M\_B\_A0  
M\_B\_A1  
M\_B\_A2  
M\_B\_A3  
M\_B\_A4  
M\_B\_A5  
M\_B\_A6  
M\_B\_A7  
M\_B\_A8  
M\_B\_A9  
M\_B\_A10  
M\_B\_A11  
M\_B\_A12  
M\_B\_A13  
M\_B\_A14  
M\_B\_A15  
-M\_B\_DQS0  
-M\_B\_DQS1  
-M\_B\_DQS2  
-M\_B\_DQS3  
-M\_B\_DQS4  
-M\_B\_DQS5  
-M\_B\_DQS6  
-M\_B\_DQS7  
M\_B\_DQS0  
M\_B\_DQS1  
M\_B\_DQS2  
M\_B\_DQS3  
M\_B\_DQS4  
M\_B\_DQS5  
M\_B\_DQS6  
M\_B\_DQS7

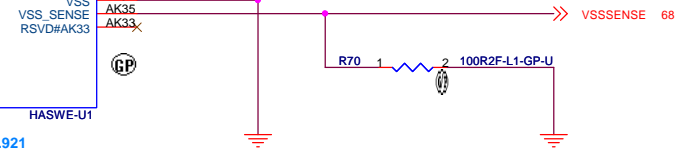
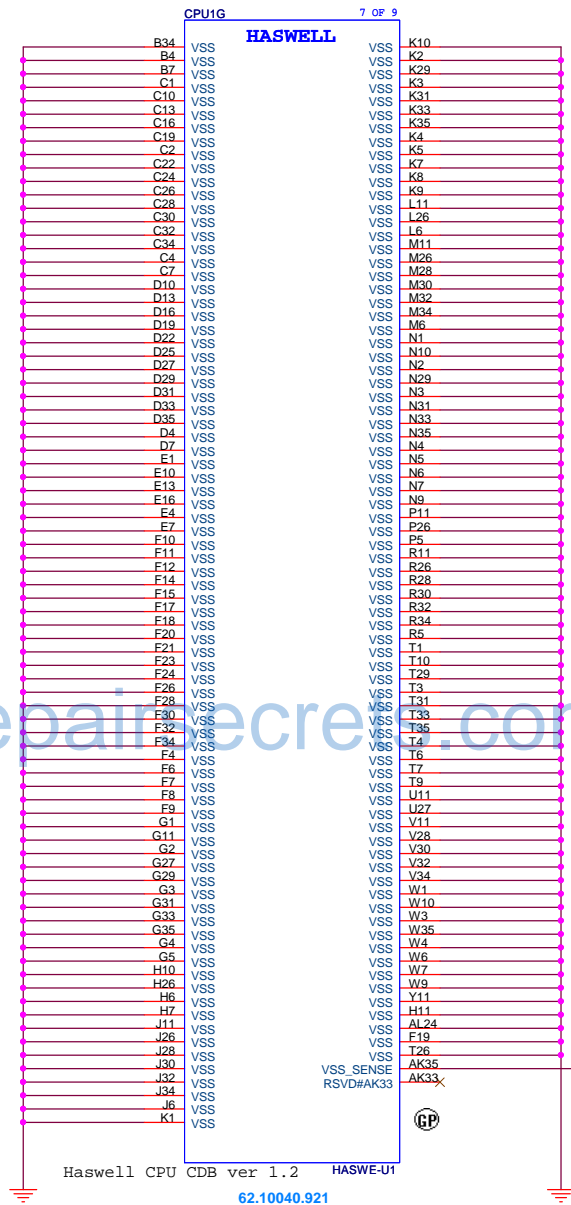
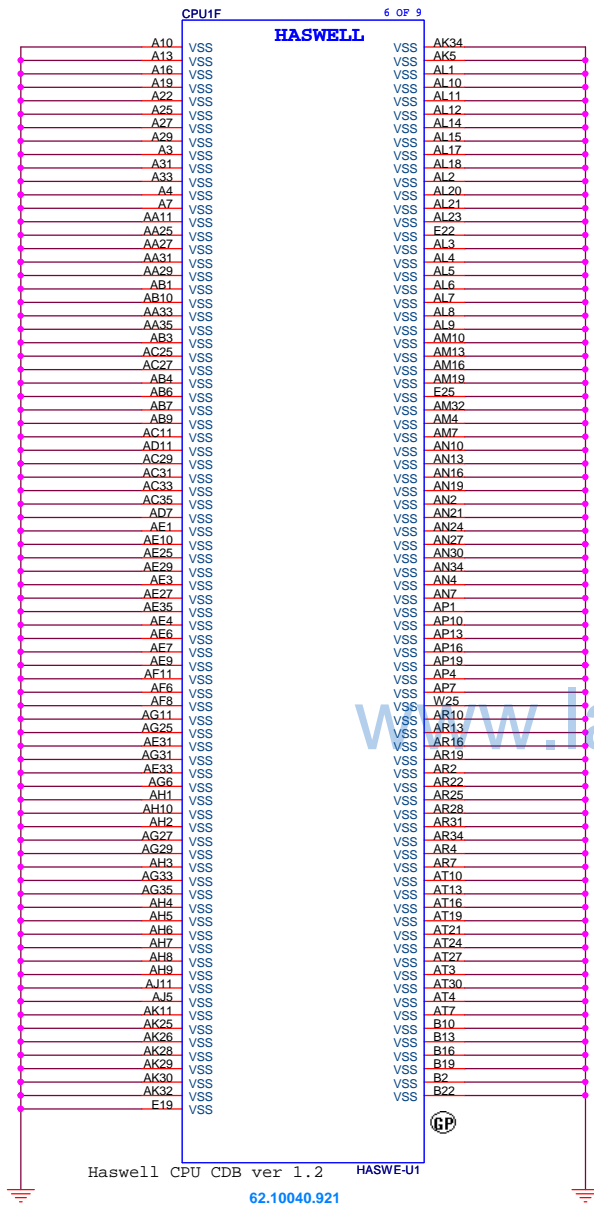
<< >> M\_B\_A[15:0] 90,91

<< >> -M\_B\_DQS[7:0] 90,91

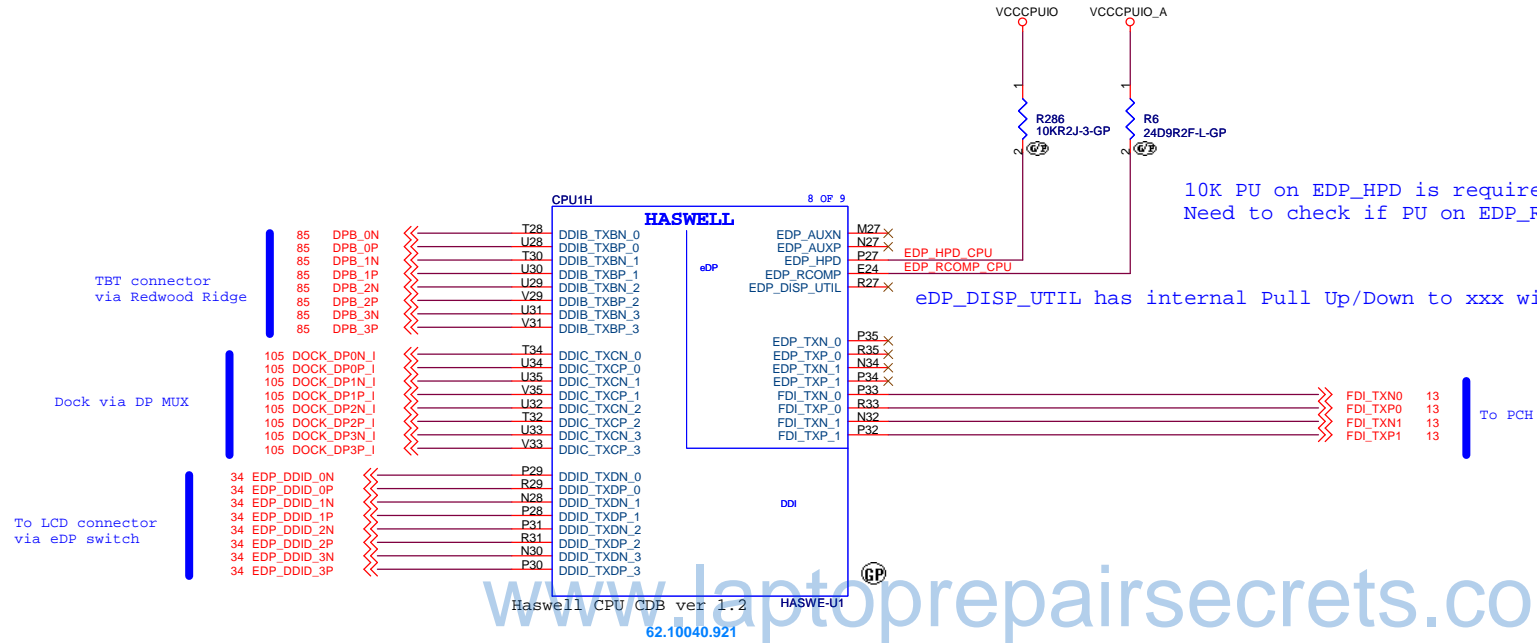
<< >> M\_B\_DQS[7:0] 90,91

Haswell CPU CDB ver 1.2 HASWE-UT  
62.10040.921









10K PU on EDP\_HPDCPU is required even Native eDP is disabled.  
Need to check if PU on EDP\_RCOMP is required.

eDP\_DISP\_UTIL has internal Pull Up/Down to xxx with 100ohm.

<Variant Name>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Haswell EDP/DDI (7/8)**

Size  
A3

Document Number

**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

Sheet 9 of 105

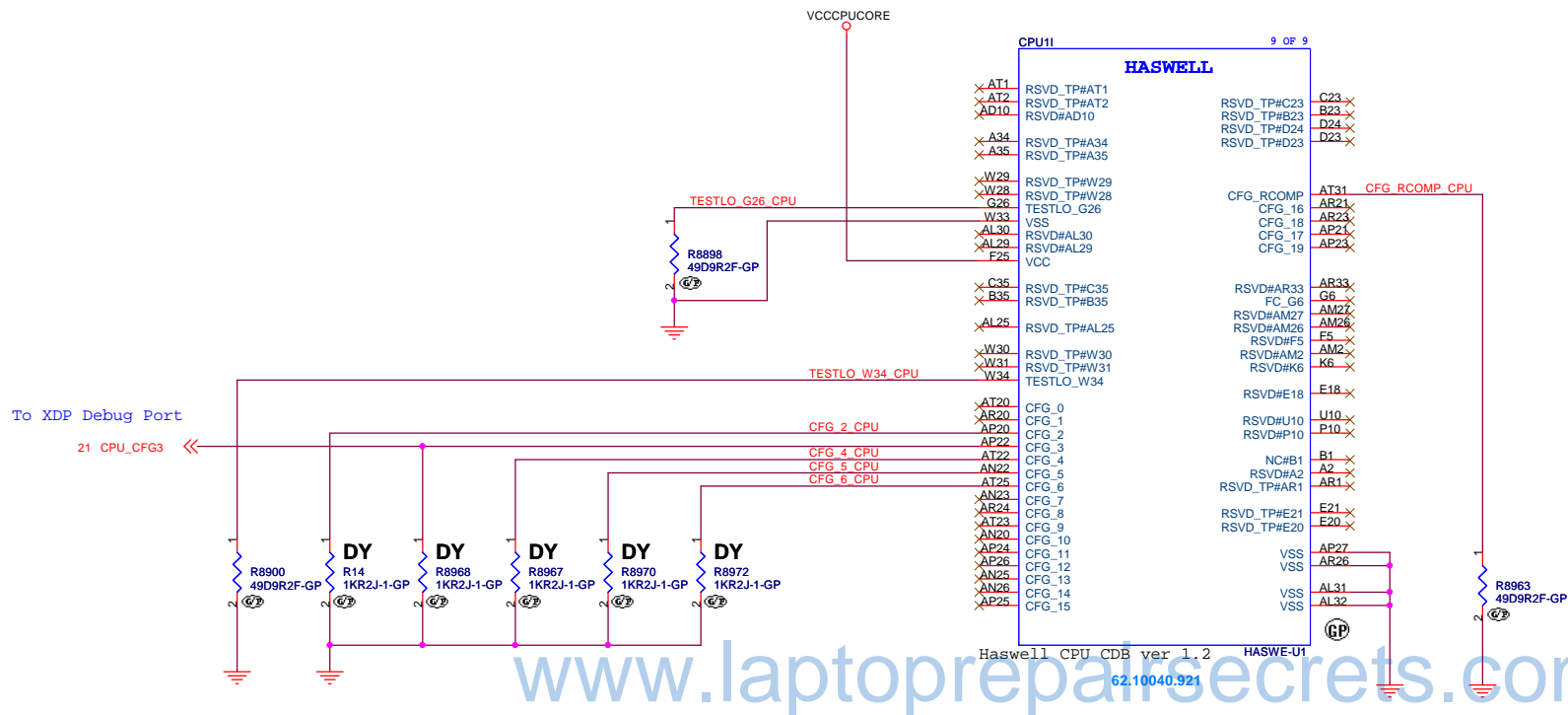


TABLE CFG[17:0] pin has inteernal Pull up to VCCIO\_OUT with 40~60ohm.

<b>CFG2 : PEG Static Lane Reversal</b> Need to confirm for SWG and WS Model	
1	: Normal Operation
0	: Lane Reversal
<b>CFG3 : MSR Privacy Bit Feature</b>	
1	: Debug capability is determined by MSR(0xC80) bit0
0	: MSR (0xC80) bit0 default setting overridden
<b>CFG4 : Display Port Presence</b>	
1	: Disabled
0	: Enabled
<b>CFG[6:5] : PEG Bifurcation</b>	
11	: Func 1 Disabled, Func 2 Disabled (x16,---,---)    WS uses x16 without Thunderbolt
10	: Func 1 Enabled, Func 2 Disabled (x8,x8,---)    UMA, SWG uses x8 & x8
01	: Func 1 Disabled, Func 2 Enabled
00	: Func 1 Enabled, Func 2 Enabled (x8,x4,x4)    WS uses x8, x4 with Thunderbolt

<Variant Name>

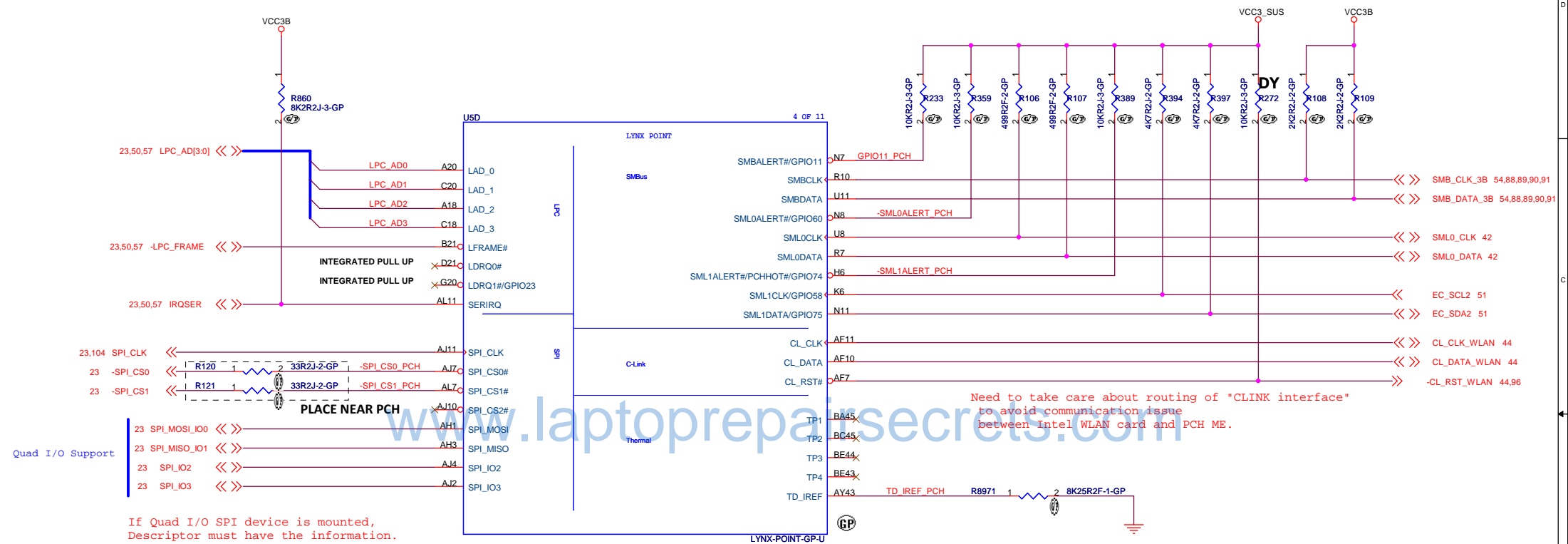
**緯創資通**    **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
**Haswell CFG/RSV (8/8)**

Size    Document Number    Rev  
A3    **Kome-1 WS**    -1

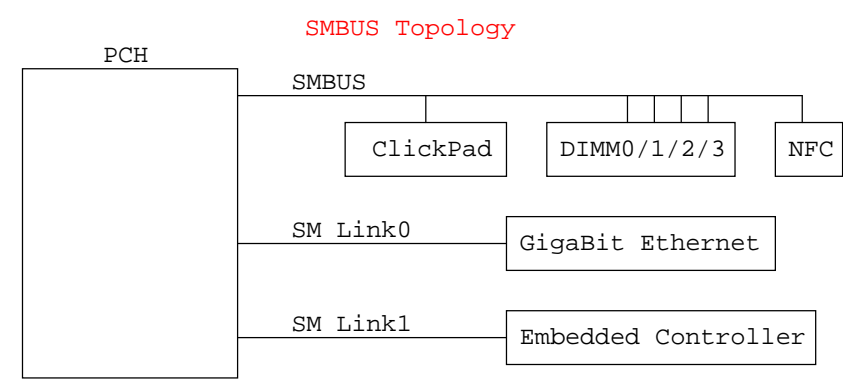
Date: Thursday, September 12, 2013    Sheet    10    of    105





Quad I/O Support

If Quad I/O SPI device is mounted,  
Descriptor must have the information.





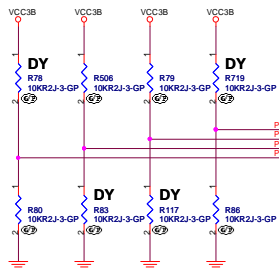
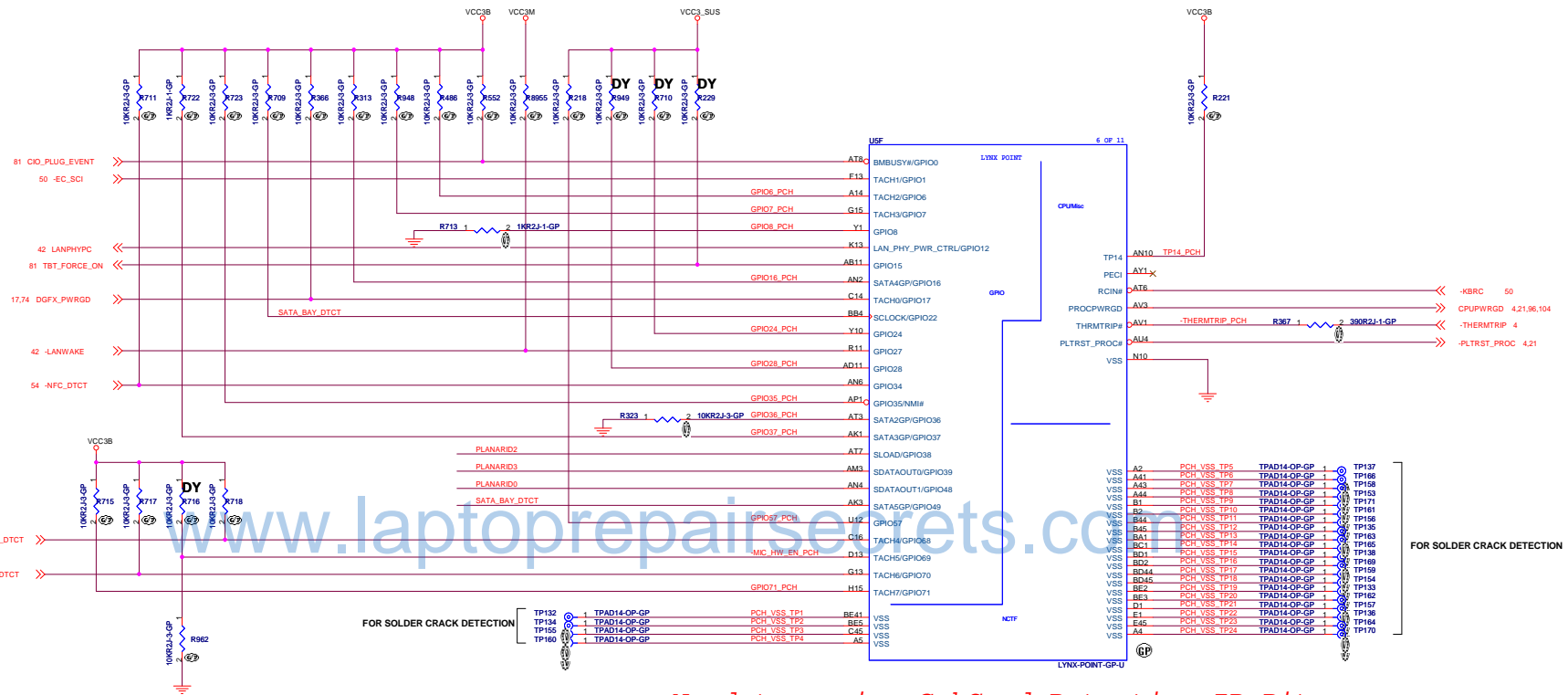


TABLE

GPIO8	INTEGRATED CLOCKING
HIGH	DISABLED(BTM)
LOW	ENABLED(FCIM)

TABLE

GPIO37	ME CRYPTO STRAP
HIGH	WITH CONFIDENTIALITY
LOW	NO CONFIDENTIALITY



TABLE

LEVEL	PLANAR ID			
	3	2	1	0
1	R78	R506	R79	R719
0	R80	R83	R117	R86

TABLE

LEVEL	PLANARID[3..0]
SDV	0000B
ME-FVT	0010B
FVT	0011B
ME-SIT	0011B
SIT	0100B
SIT-R	0101B
SVT	0110B

&lt;Variant Name&gt;

緯創資通 Wistron Corporation	
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.	
Title LynxPoint GPIO (5/10)	
Size A2	Document Number Kome-1 WS
Date: Thursday, September 12, 2013	Sheet 15 of 106

Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1 (System Port)	USB3P1_SYSP0
Port 2	USB3 2	USB3 2 (System Port)	USB3P2_SYSP1
Port 3	USB3 5	USB3 5 (Docking Port)	USB3P5_DOCK
Port 4	USB3 6	USB3 6 (Reserved)	NC
Port 5	PCIE 1/USB3 3	PCIE 1 (Media Card)	PCIEP1_MEDIACARD
Port 6	PCIE 2/USB3 4	PCIE 2 (NGFF_WLAN)	PCIEP2_NGFF_WLAN
Port 7	PCIE 3	PCIE 3 (Express slot)	PCIEP3_EXP_SLOT
Port 8	PCIE 4	PCIE 4 (GbE)	PCIEP4_GBE
Port 9	PCIE 5	PCIE 5 (Thunderbolt)	PCIEP5_THUNDER_L0
Port 10	PCIE 6	PCIE 6 (Thunderbolt)	PCIEP6_THUNDER_L1
Port 11	PCIE 7	PCIE 7 (Thunderbolt)	PCIEP7_THUNDER_L2
Port 12	PCIE 8	PCIE 8 (Thunderbolt)	PCIEP8_THUNDER_L3
Port 13	SATA 4/PCIE 1	SATA 4 (NGFF_WWAN)	SATAP4_NGFF_WWAN
Port 14	SATA 5/PCIE 2	SATA 5 (ODD Bay)	SATAP5_ODD_BAY
Port 15	SATA 0	SATA 0 (HDD Bay)	SATAP0_HDD_BAY
Port 16	SATA 1	SATA 1 (NGFF_SSD)	SATAP1_NGFF_SSD
Port 17	SATA 2	SATA 2 (Reserved)	NC
Port 18	SATA 3	SATA 3 (Reserved)	NC

PCIe Port Assignment	
1	Media Card Controller
2	NGFF WLAN Slot
3	Express Slot
4	GbE PHY
5	Thunderbolt Lane0
6	Thunderbolt Lane1
7	Thunderbolt Lane2
8	Thunderbolt Lane3

USB 3.0 Port Assignment	
1	USB 3.0 System Port 0
2	USB 3.0 System Port 1 (Debug)
3	Reserved
4	Reserved
5	USB 3.0 Docking IF
6	Reserved

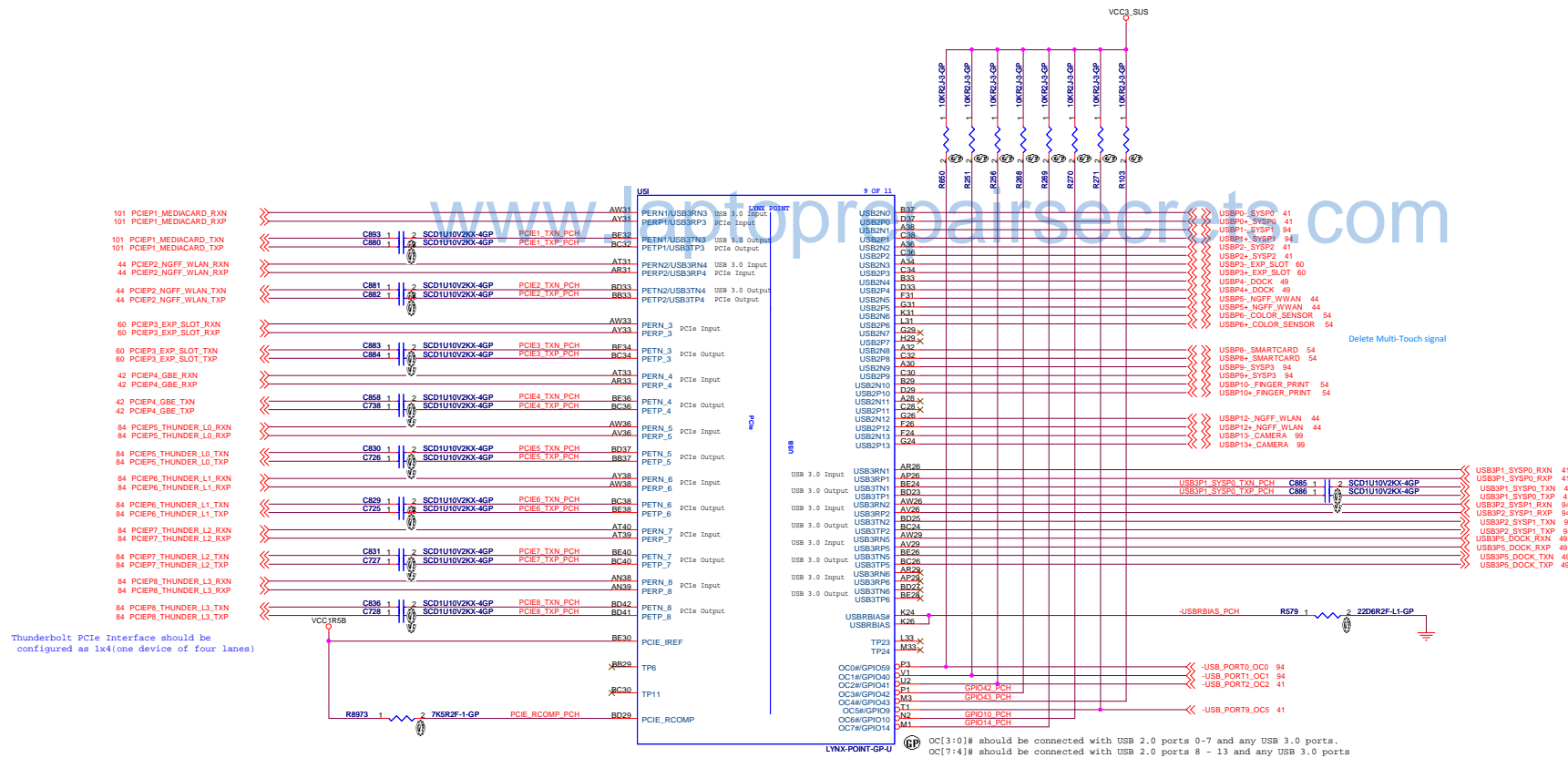
USB Port Assignment	
0	USB 2.0 System Port 0
1	USB 2.0 System Port 1 (Debug)
2	USB 2.0 System Port 2 (AOU)
3	Express Slot
4	USB 2.0 Docking
5	NGFF WWAN Slot
6	Color Sensor [WS Model only]
7	Reserved
8	Smart Card Slot
9	USB 2.0 System Port3
10	Fingerprint Reader
11	Reserved
12	NGFF WLAN Slot (Bluetooth)
13	USB Camera in LCD

SATA Port Assignment	
0	HDD Connector
1	NGFF SSD Slot
2	Reserved
3	Reserved
4	NGFF WWAN Slot
5	ODD Bay Connector

Soft Strap in Flash descriptor:

PCHSTRP4 bit 3,2 [SATA Port 5 PCIe Port 2 Mode]  
00 = Assigned to SATA Port 5 [ODD Bay]

PCHSTRP9 bit 31,30 [SATA Port 4 PCIe Port 1 Mode]  
00 = Assigned to SATA Port 4 [NGFF SSD]  
PCHSTRP9 bit 21,20 [USB3 Port 3 PCIe Port 2 Mode]  
00 = Assigned to PCIe Express [NGFF WLAN]  
PCHSTRP9 bit 19,18 [USB3 Port 2 PCIe Port 1 Mode]  
00 = Assigned to PCIe Express [MediaCard Reader]  
PCHSTRP9 bit 11 [Intel PHY Over PCI Express Enable]  
1 = PCI Express port is used by Intel PHY.  
PCHSTRP9 bit 10-8 [Intel PHY PCIe Port Select]  
011 = Port 4  
PCHSTRP9 bit 5 [PCIe Lane Reversal 2]  
0 = PCIe Lanes 4-7 are not reversed. [Thunderbolt]  
PCHSTRP9 bit 4 [PCIe Lane Reversal 1]  
0 = PCIe Lanes 0-3 are not reversed.  
PCHSTRP9 bit 3,2 [PCI Express Port Configuration Strap 2]  
11 = 1x4 Port 5 (x4), Port 6-8 (Disabled)  
PCHSTRP9 bit 1,0 [PCI Express Port Configuration strap 1]  
00 = 4x1 Ports 1-4 (x1)



OC[3:0]# should be connected with USB 2.0 ports 0-7 and any USB 3.0 ports.  
OC[7:4]# should be connected with USB 2.0 ports 8 - 13 and any USB 3.0 ports

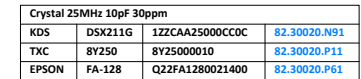
USB Port 0 on Left side has  
USB 2.0 Port 0 and USB 3.0 Port 1  
USB Port 1 on Left side has  
USB 2.0 Port 1 and USB 3.0 Port 2  
USB Port 2 on Right side has  
USB 2.0 Port 2 only  
USB Port 3 on Right side has  
USB 2.0 Port 9 only

<Variant Name>

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.	
File	<b>LynxPoint PCIe/USB (610)</b>
Size	Document Number
A2	Kome-1 WS
Date: Thursday, September 12, 2013	Sheet 16 of 106

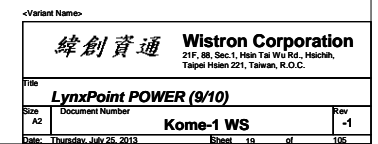


All of Switches to prevent leak on CLKREQ#  
are placed on device side to find the error.

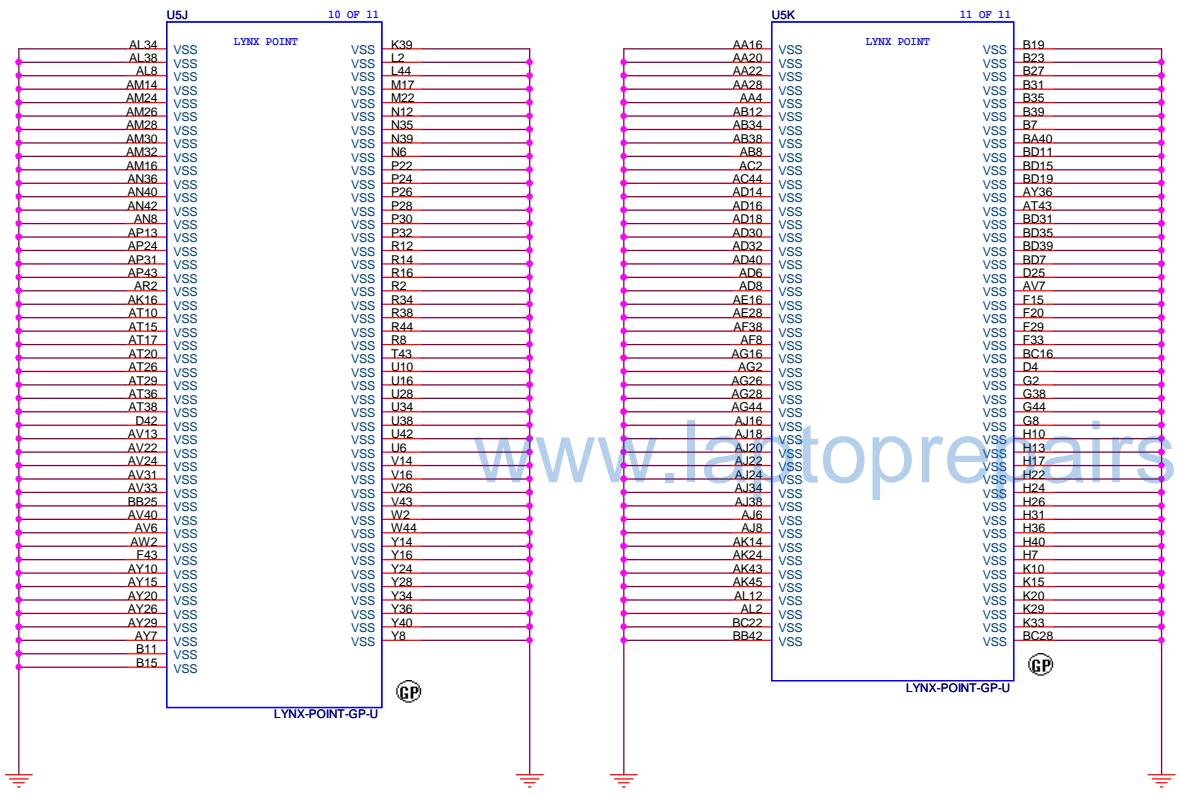


XTAL\_25M\_IN\_PCH R134 1 **DY** 2 0R2J-2-GP << PCH\_25M\_OSC\_OUT 103

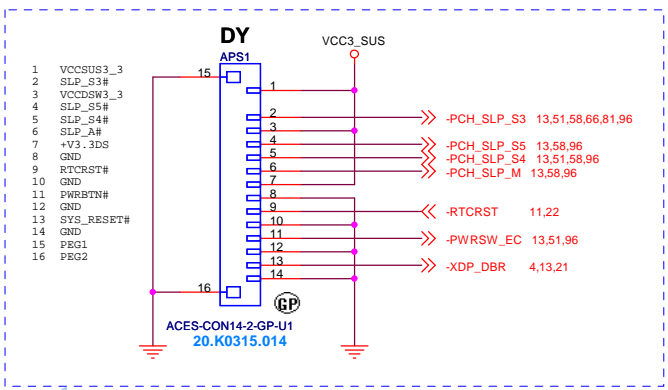




TEST PAD FOR METS/APS



APS interface for the Software ME validation



13,58 AC\_PRESENT >> TPAD14-OP-GP 1 TP11

TCK has external Pulldown(51ohm) on CPU page.  
TMS and TDI has internal pull up in CPU Module.  
TDO should have external pullup(51ohm) near Debug port.  
TRST# should have external pulldown(51ohm) near debug port.  
HOOK7(DBR) needs to connect to PCH\_SYS\_RESET# with xternal pullup.  
HOOK6(RESET#) needs to connect to RESET# with 1K series.  
HOOK3 needs to connect to PCH\_SYS\_PWROK.  
HOOK2 needs to connect to PWR\_DEBUG in CPU with external pullup(150ohm).  
HOOK1 is optional  
HOOK0(PWRGOOD) needs to connect system power good. with 1K series.  
OBSDATA\_A[3] must be connected to CPU CFG[3].

## XDP-SFF-26pin Interface

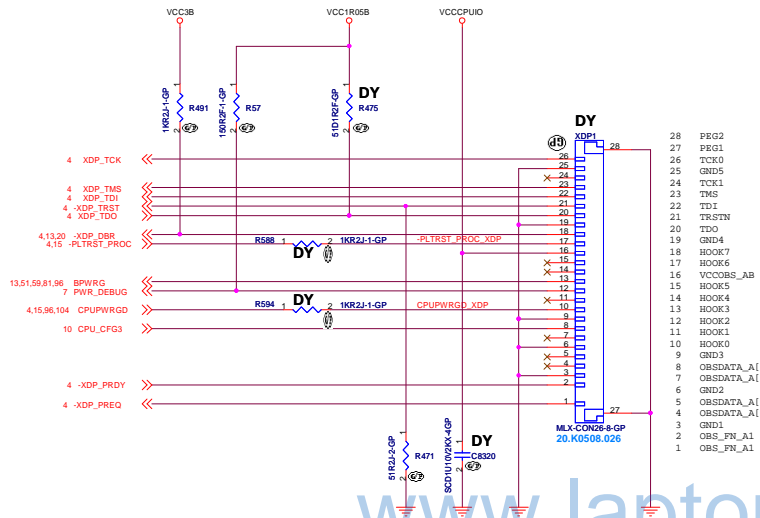


TABLE NOTE: XDP1 "ASM" FOR PDV/SDV ONLY.

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R475	ASM	NO ASM
TRST#	R471	ASM	ASM
DBRST#	R491	ASM	ASM
RESET#	R588	ASM	NO ASM
PWRGD	R594	ASM	NO ASM
PWR_DEBUG	R57	ASM	ASM
XDP1.P16	C8320	ASM	NO ASM
	XDP1	ASM	NO ASM

↑  
LOGIC

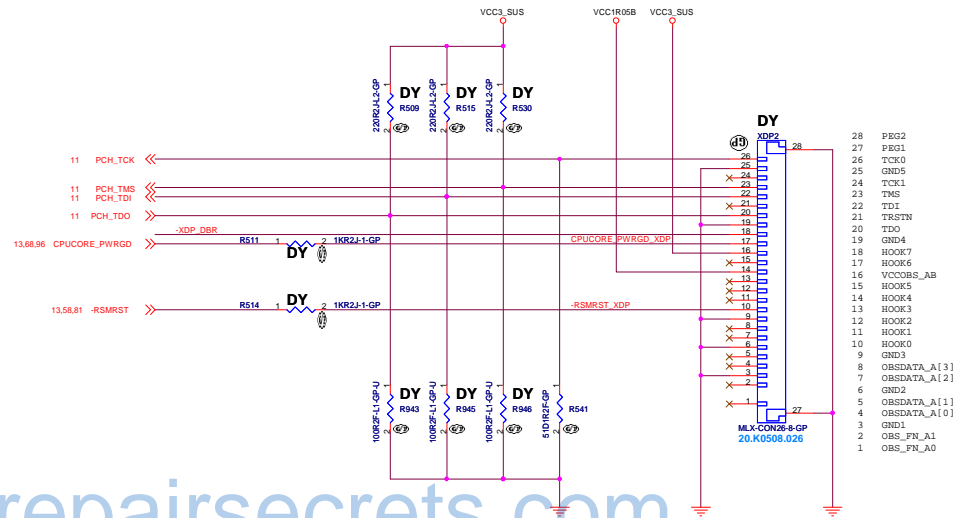


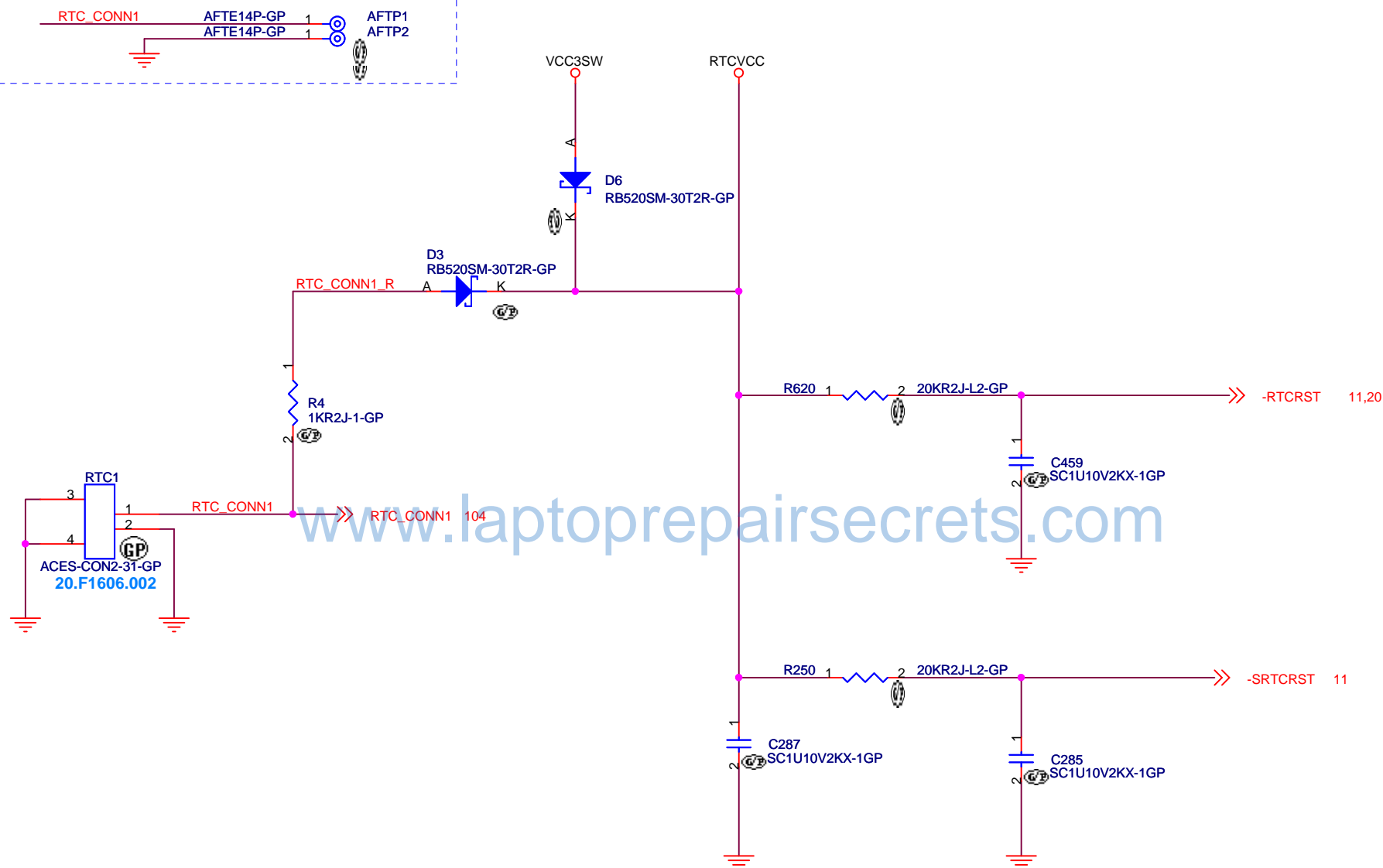
TABLE NOTE: XDP2 "ASM" FOR PDV/SDV ONLY.

SIGNAL	REF DES	ENABLE	DISABLE
TDO	R509	220	NO ASM
	R943	100	NO ASM
TMS	R530	220	NO ASM
	R946	100	NO ASM
TDI	R515	220	NO ASM
	R945	100	NO ASM
TCK	R541	51	51
CPUCORE_PWRGD	R511	ASM	NO ASM
-RSMRST	R514	ASM	NO ASM
	XDP2	ASM	NO ASM

↑  
LOGIC

<Variant Name>

Near RTC BAT CONN: RTC1 (p.022)

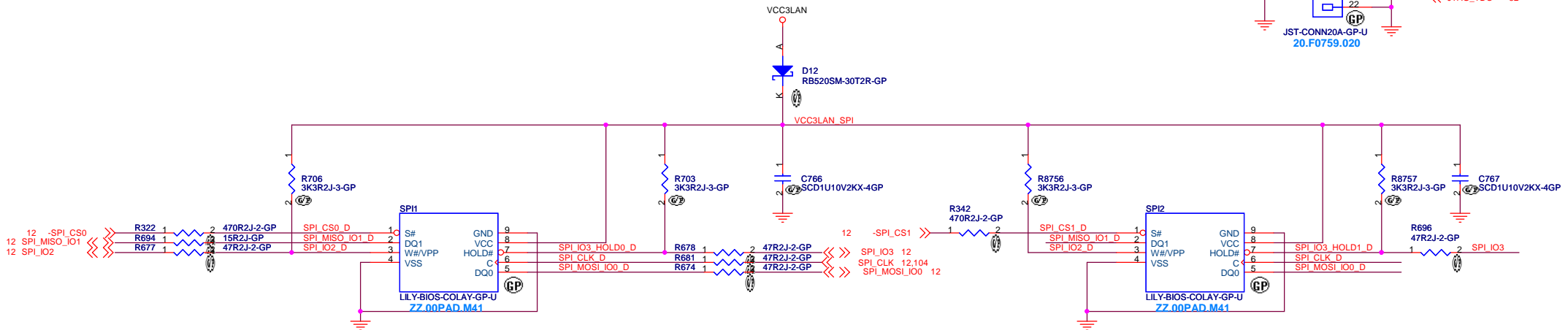
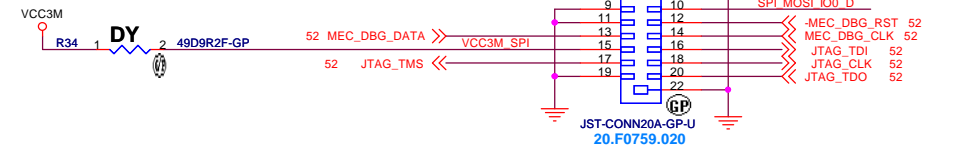


<Variant Name>

<b>緯創資通</b>			<b>Wistron Corporation</b>		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>RTC BATTERY</b>					
Size	Document Number				Rev
A4	<b>Kome-1 WS</b>				<b>-1</b>
Date: Thursday, September 12, 2013			Sheet 22 of 105		

# Trace FIFO debug port

	Enable	Disable
R34	ASM	NO ASM



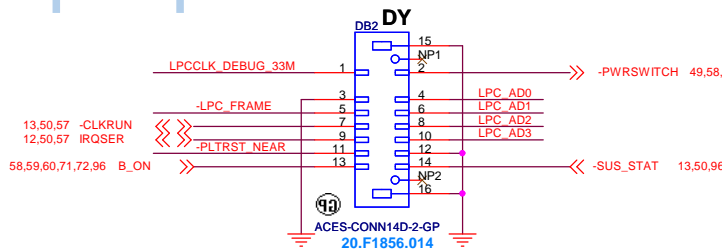
64Mbits SPI FLASH (SPI1) : 4 I/O Support SPI Flash should be applied.

Package	Supplier	Vendor P/N	Lenovo P/N	Wistron P/N
SO8	Macronix	MX25L6473EM2I-10G		72.25647.00A
	Winbond	W25Q64FVSSIQ		72.25Q64.K01
	Eon	EN25QH64-104HIP Rev.F		72.02564.001
	Micron	N25Q064A13ESEC0F		72.25Q64.G01

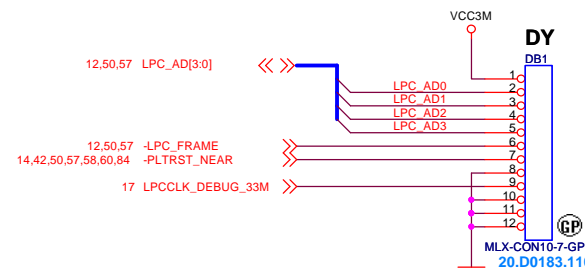
32Mbits SPI FLASH (SPI2) : 4 I/O Support SPI Flash should be applied.

Package	Supplier	Vendor P/N	Lenovo P/N	Wistron P/N
SO8	Macronix	MX25L3273EM2I-10G		72.25327.A01
	Winbond	W25Q32FVSSIQ		72.25Q32.H01
	Eon	EN25QH32-104HIP Rev.F		72.02532.B01
	Micron	N25Q032A13ESEC0F		72.25Q32.C01

## Lenovo Debug Tool I/F



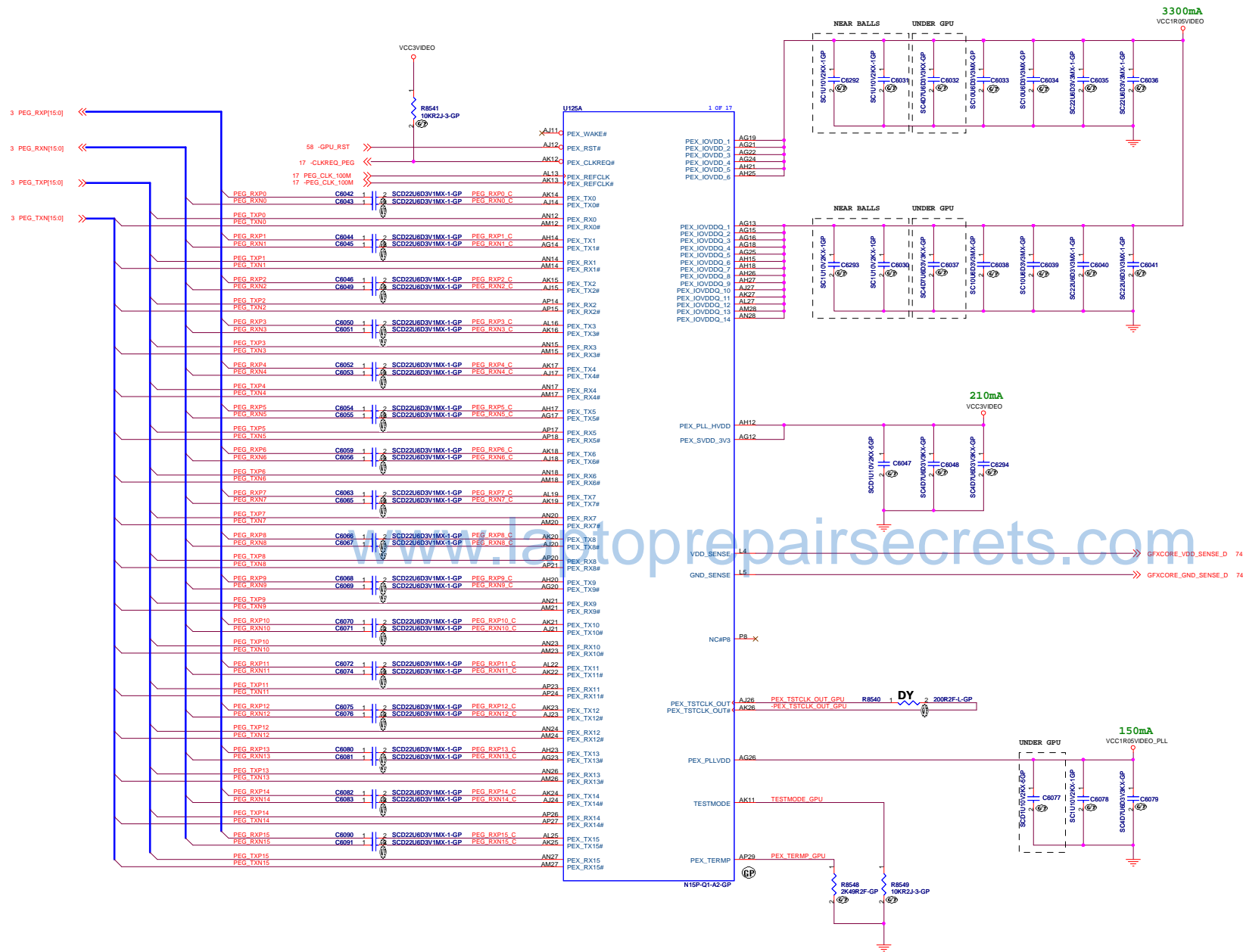
## LPC for Debug Card Connector



<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

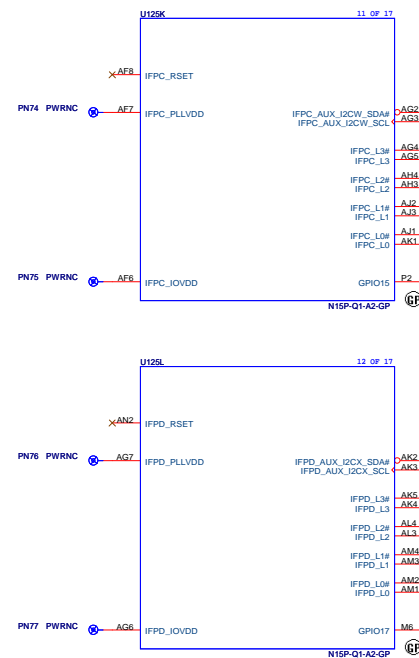
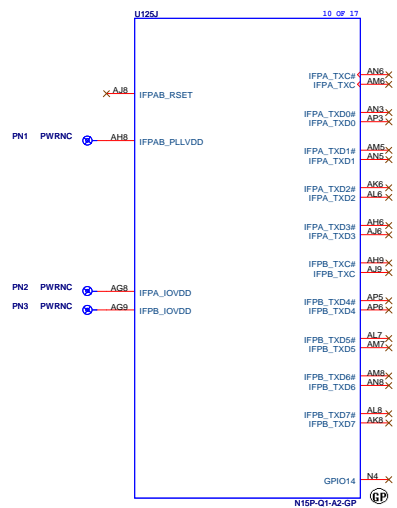
Title	SPI Flash, DEBUG PORT		
Size	Document Number	Kome-1 WS	Rev -1
Date	Thursday, September 12, 2013	Sheet 23	of 105



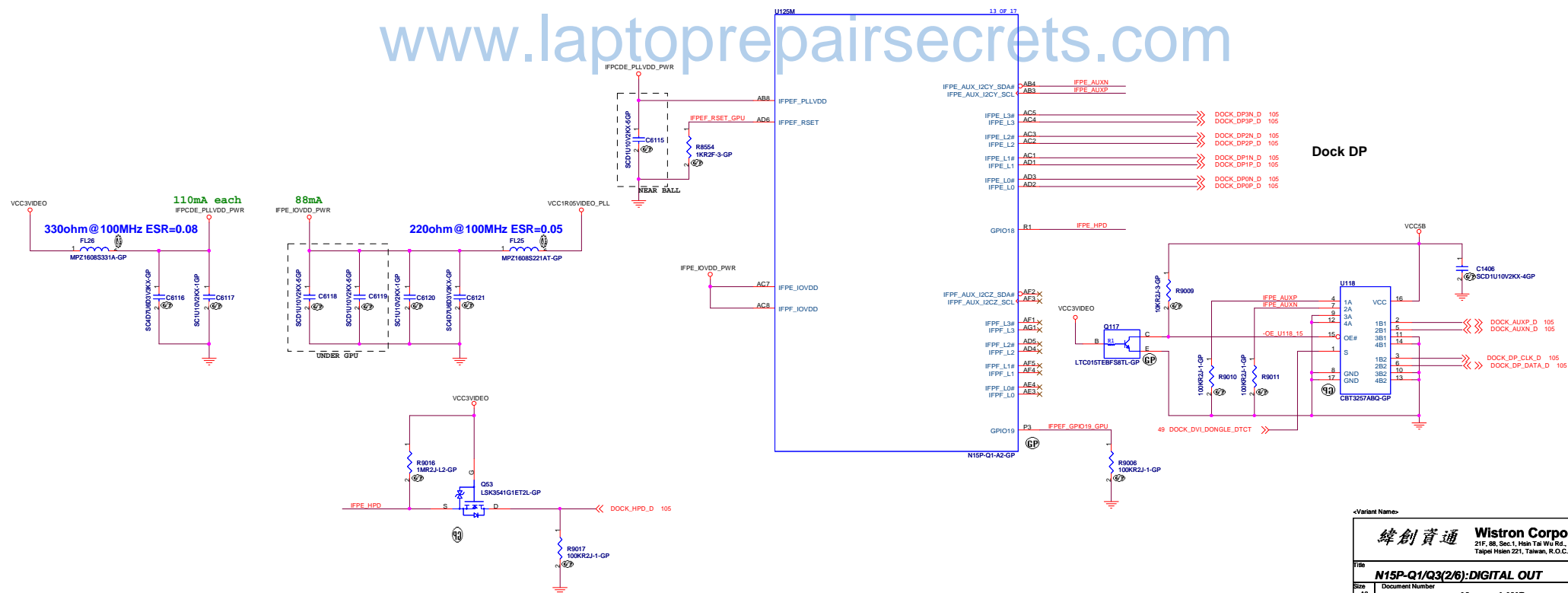
<Variant Name>

緯創資通 Wistron Corporation	
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsueh-shan, Taipei Hsien 221, Taiwan, R.O.C.	
File N15P-Q1/Q3(1/6):PEG I/F	
Size A2	Document Number Kome-1 WS
Date: Thursday, September 12, 2013	Sheet 24 of 106



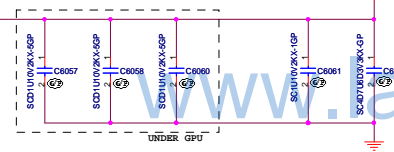
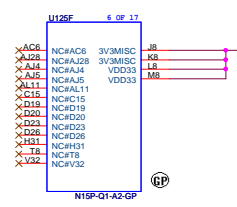
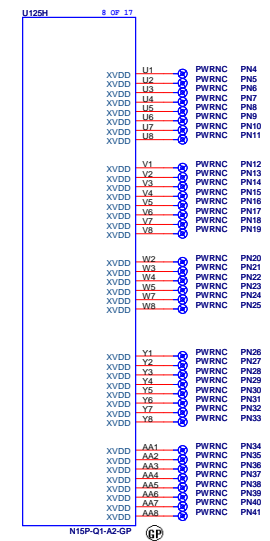
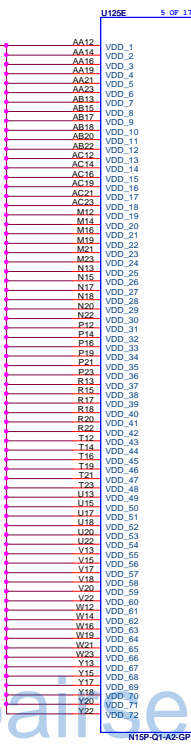
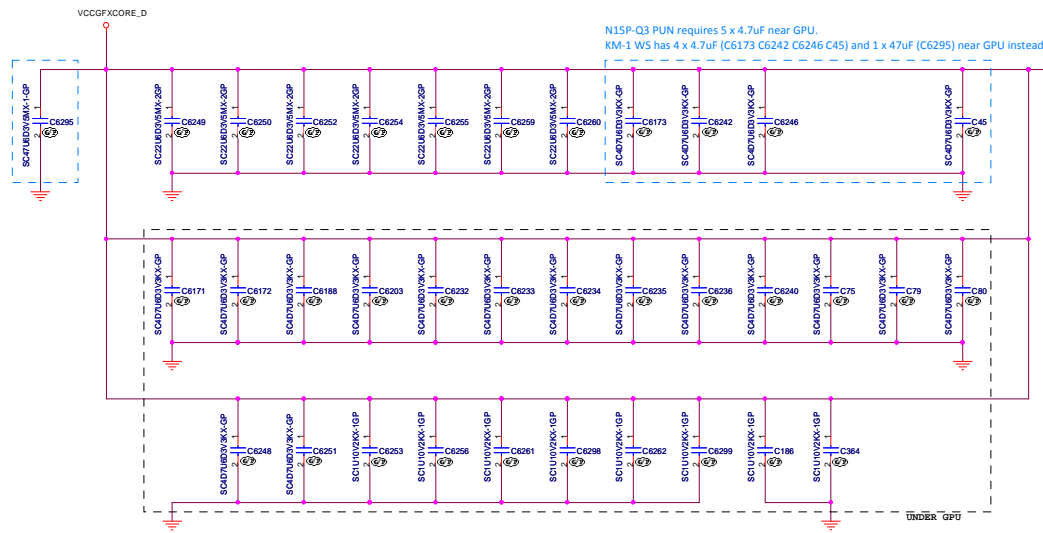


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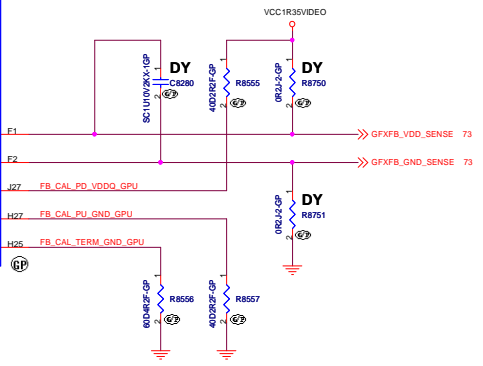
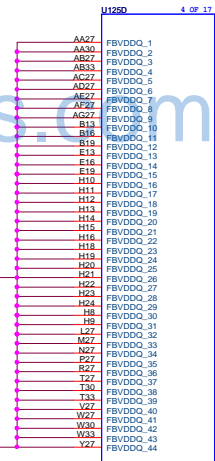
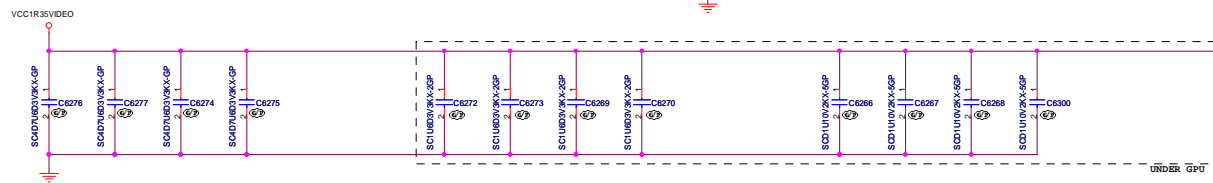
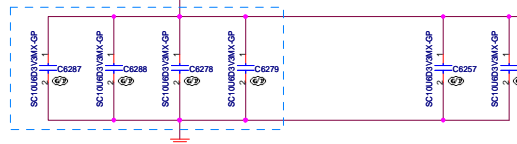


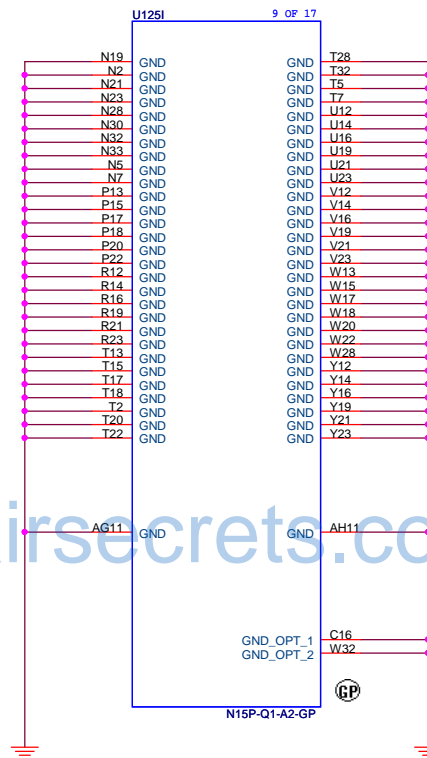
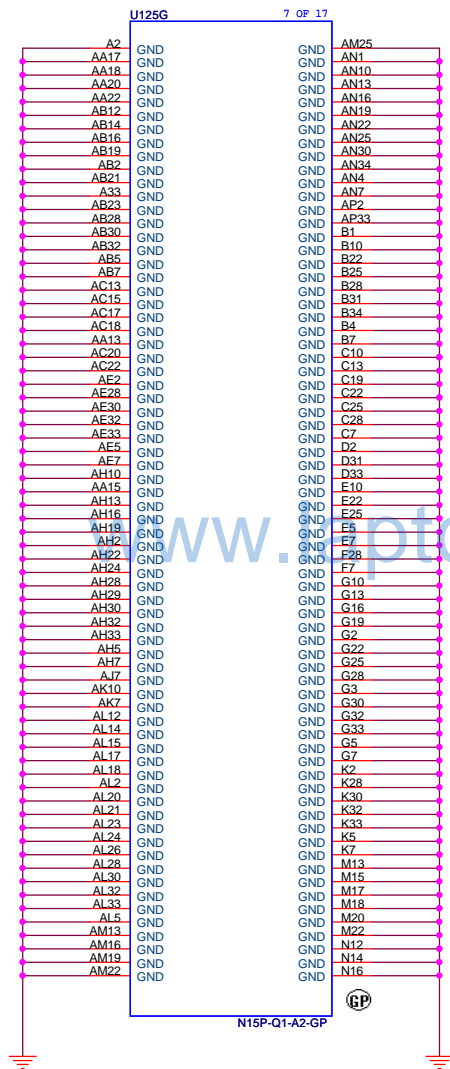






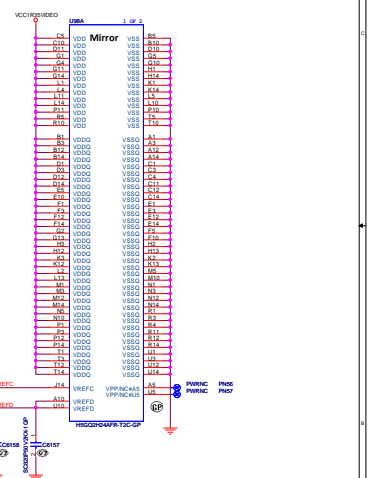
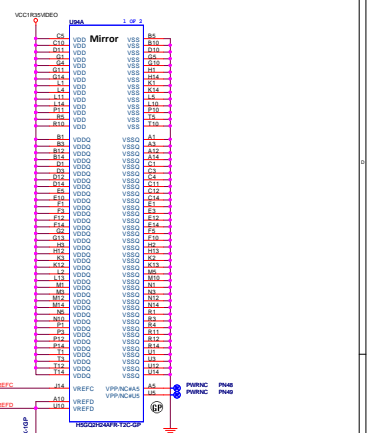
Power Team Request:  
From two 22uF 0805 to four 10uF 0603



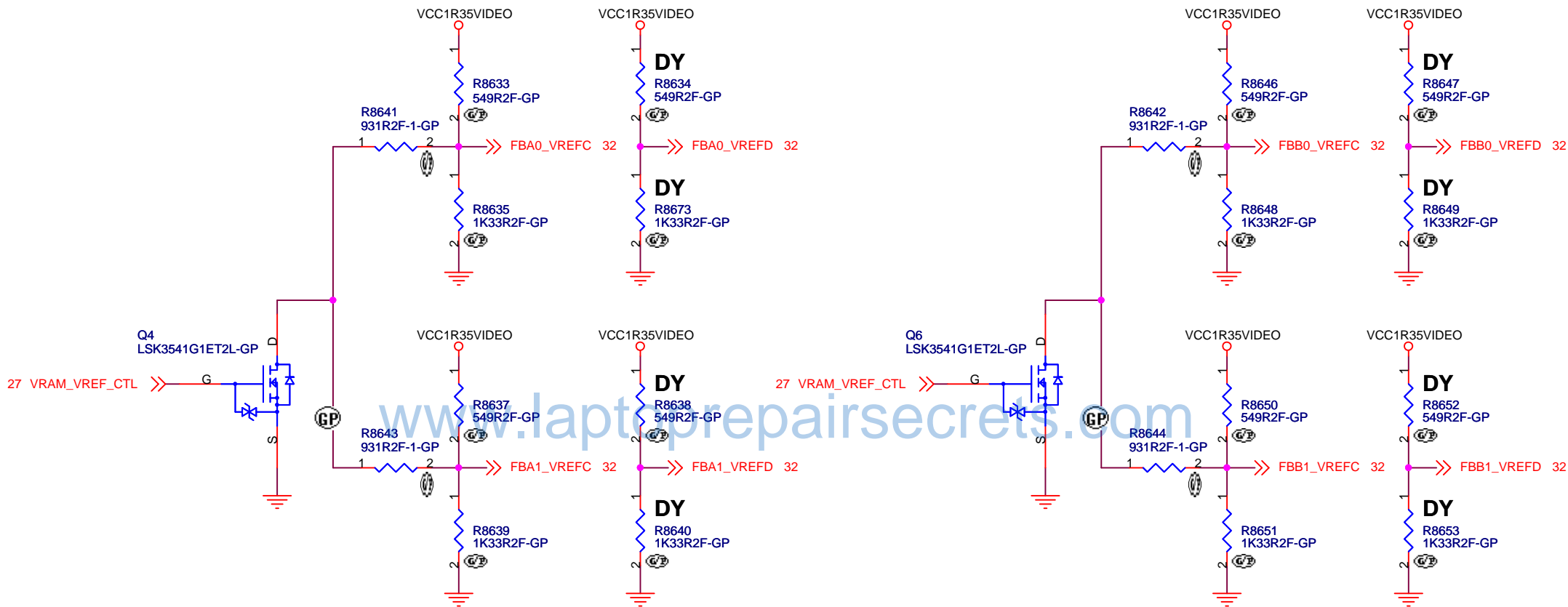












<Variant Name>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**MEMORY TERMINATION**

Size  
A4

Document Number

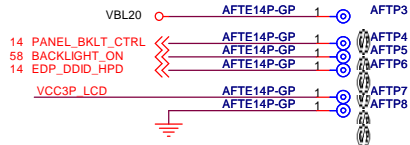
**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

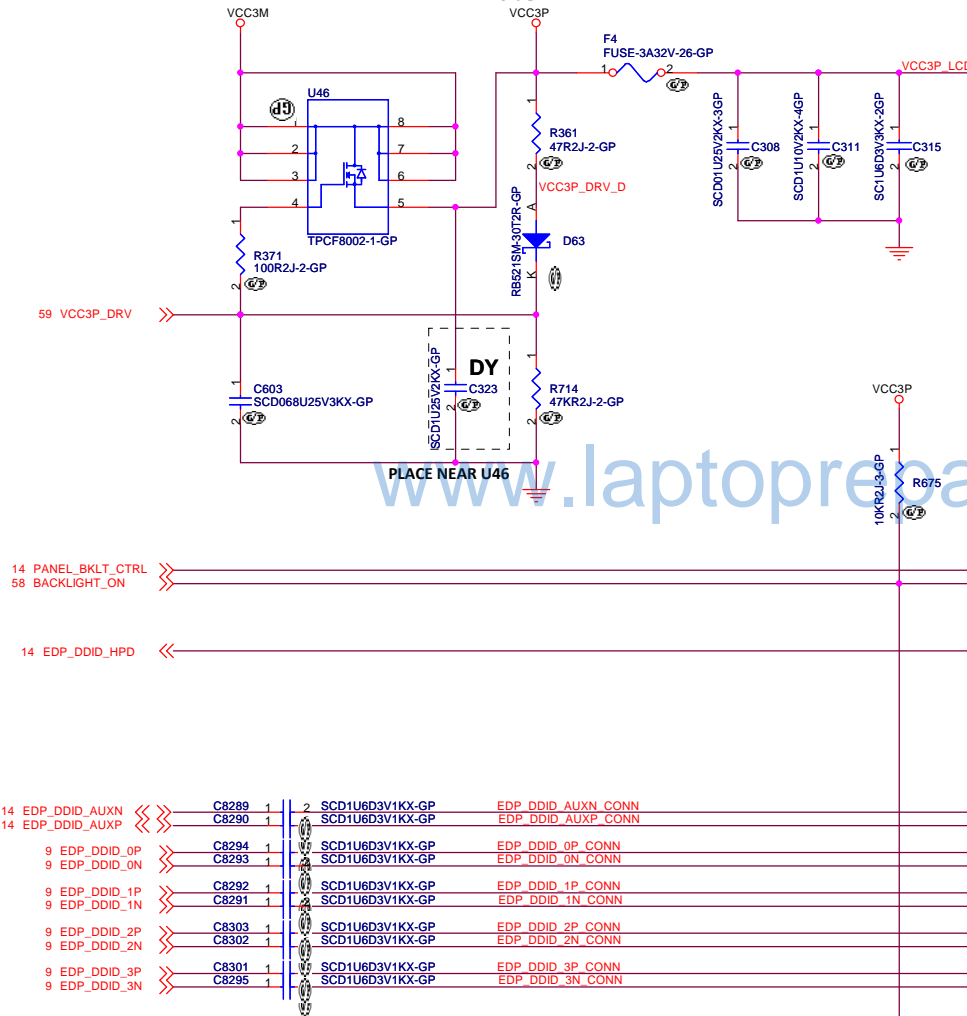
Sheet 33 of 105

# Near LCD CONN: LCD1 (p.034)



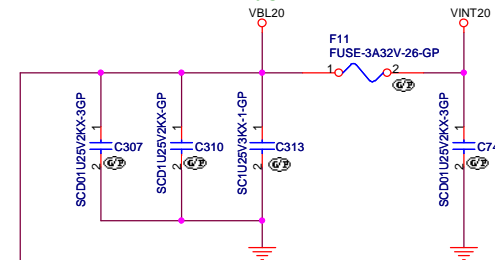
Max Average Current 0.9A @ 3.0V

0.9A



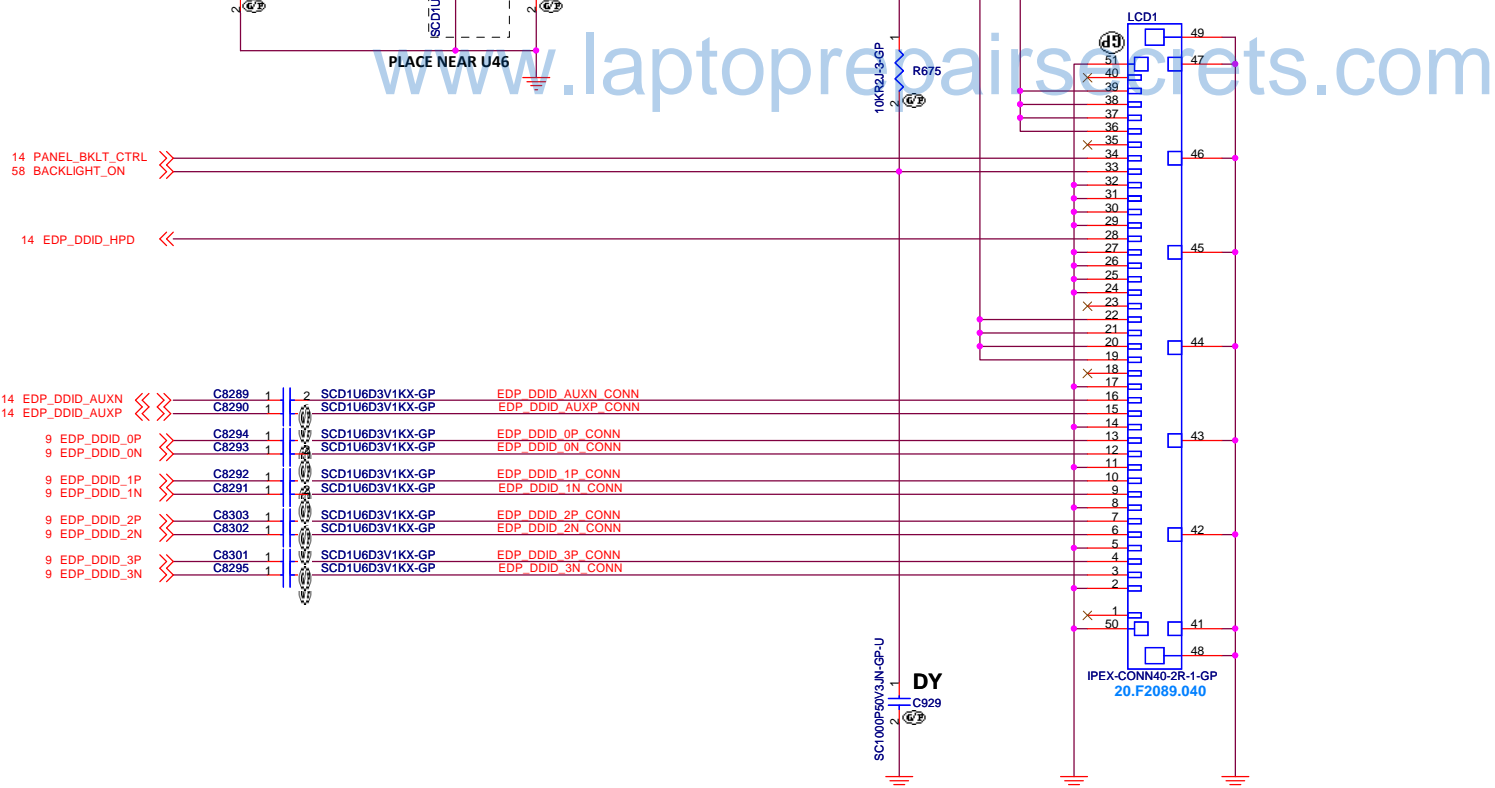
Max Average Current 1.3A @ 6.0V

1.3A



Support FHD++ panel

## LCD CONNECTOR



<Variant Name>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LCD CONNECTOR		
Size	Document Number	Rev
A3	Kome-1 WS	-1
Date: Thursday, September 12, 2013 Sheet 34 of 105		

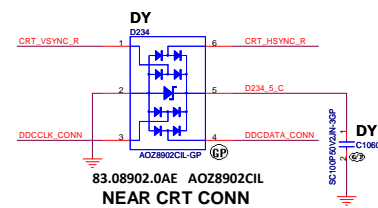
www.laptoprepairssecrets.com

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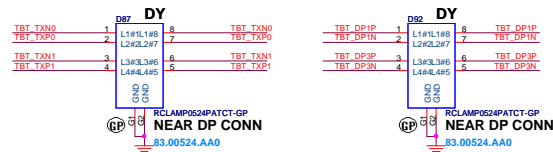
<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
BLANK		
Size	Document Number	Rev
A4	Kome-1 WS	-1
Date: Wednesday, July 17, 2013		Sheet 35 of 105

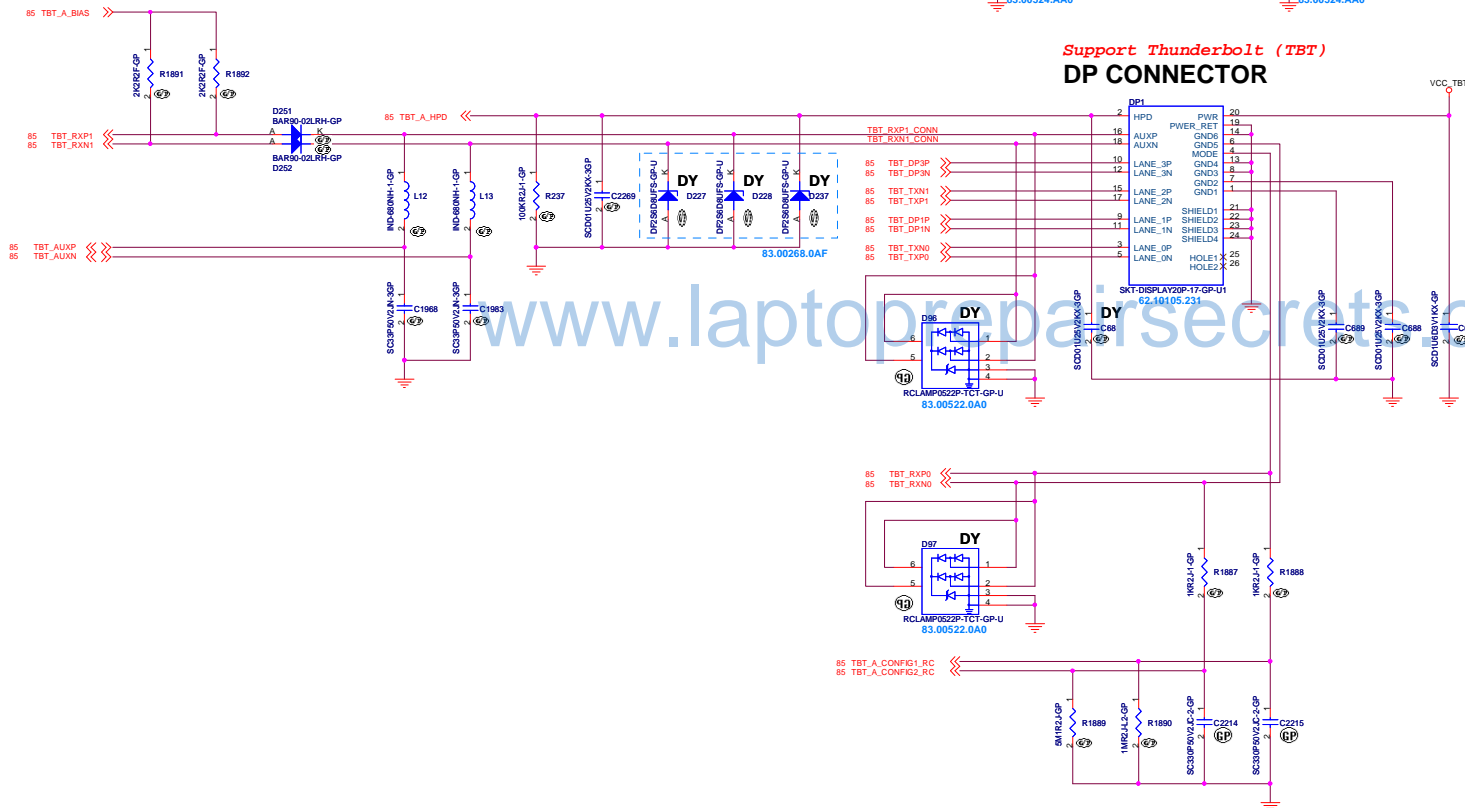
Signal Name	Connector Pin	Board Pin
CRT_VCC5V_CONN	1	AFTF14P-GP 1
CRT_RED_CONN	2	AFTF14P-GP 2
CRT_GREEN_CONN	3	AFTF14P-GP 3
CRT_BLUE_CONN	4	AFTF14P-GP 4
CRT_VSYNC_CONN	5	AFTF14P-GP 5
CRT_HSYNC_CONN	6	AFTF14P-GP 6
DDCDATA_CONN	7	AFTF14P-GP 7
DDCCLK_CONN	8	AFTF14P-GP 8
	9	AFTF14P-GP 9 (Ground)
	10	AFTF14P-GP 10
	11	AFTF14P-GP 11
	12	AFTF14P-GP 12
	13	AFTF14P-GP 13
	14	AFTF14P-GP 14



# Near THUNDERBOLT CONN: DP1 (p.037)



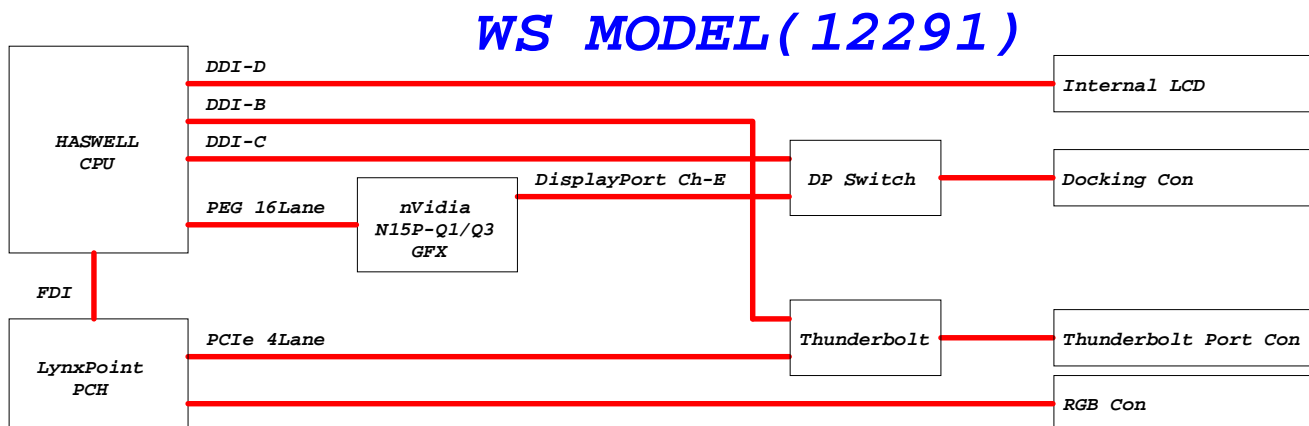
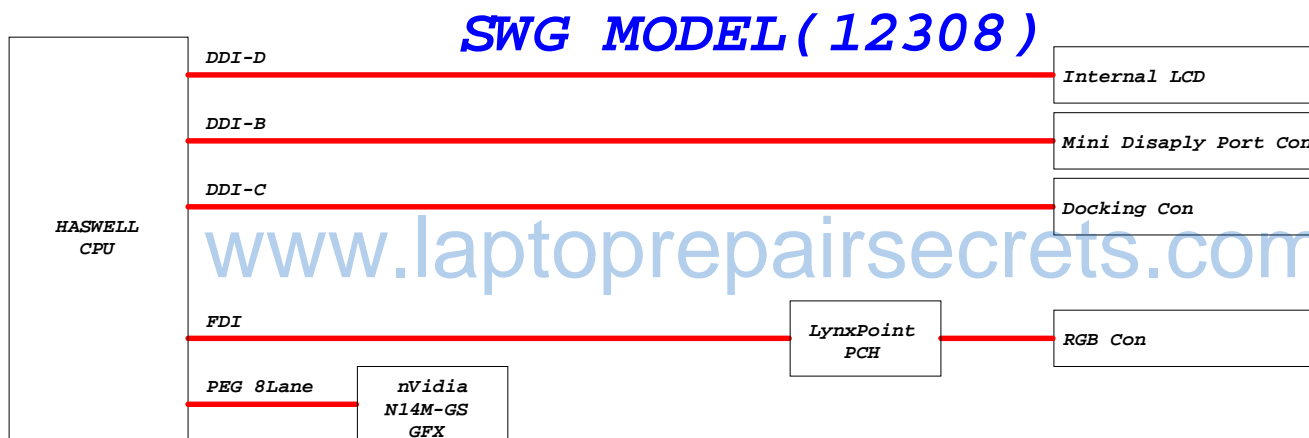
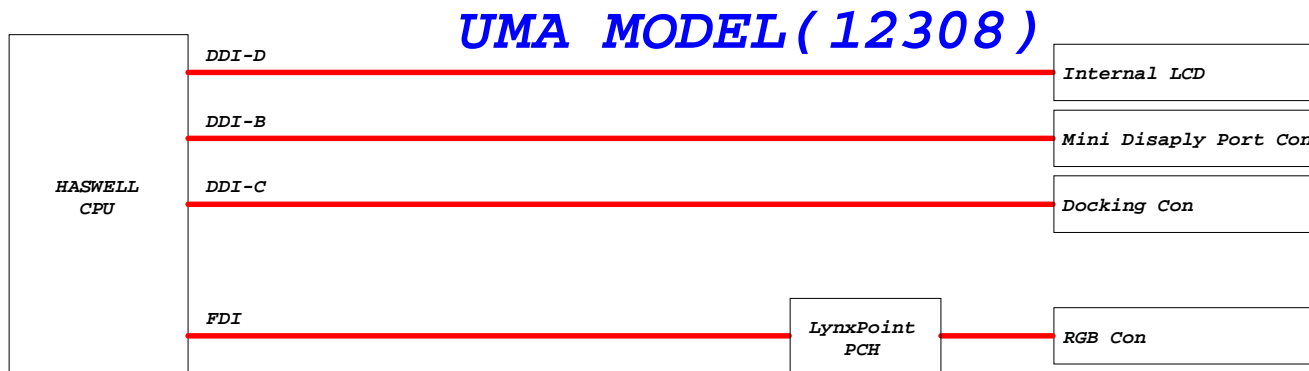
## Support Thunderbolt (TBT) DP CONNECTOR



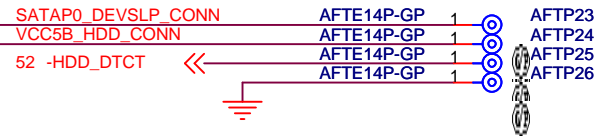
<Variant Name>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.

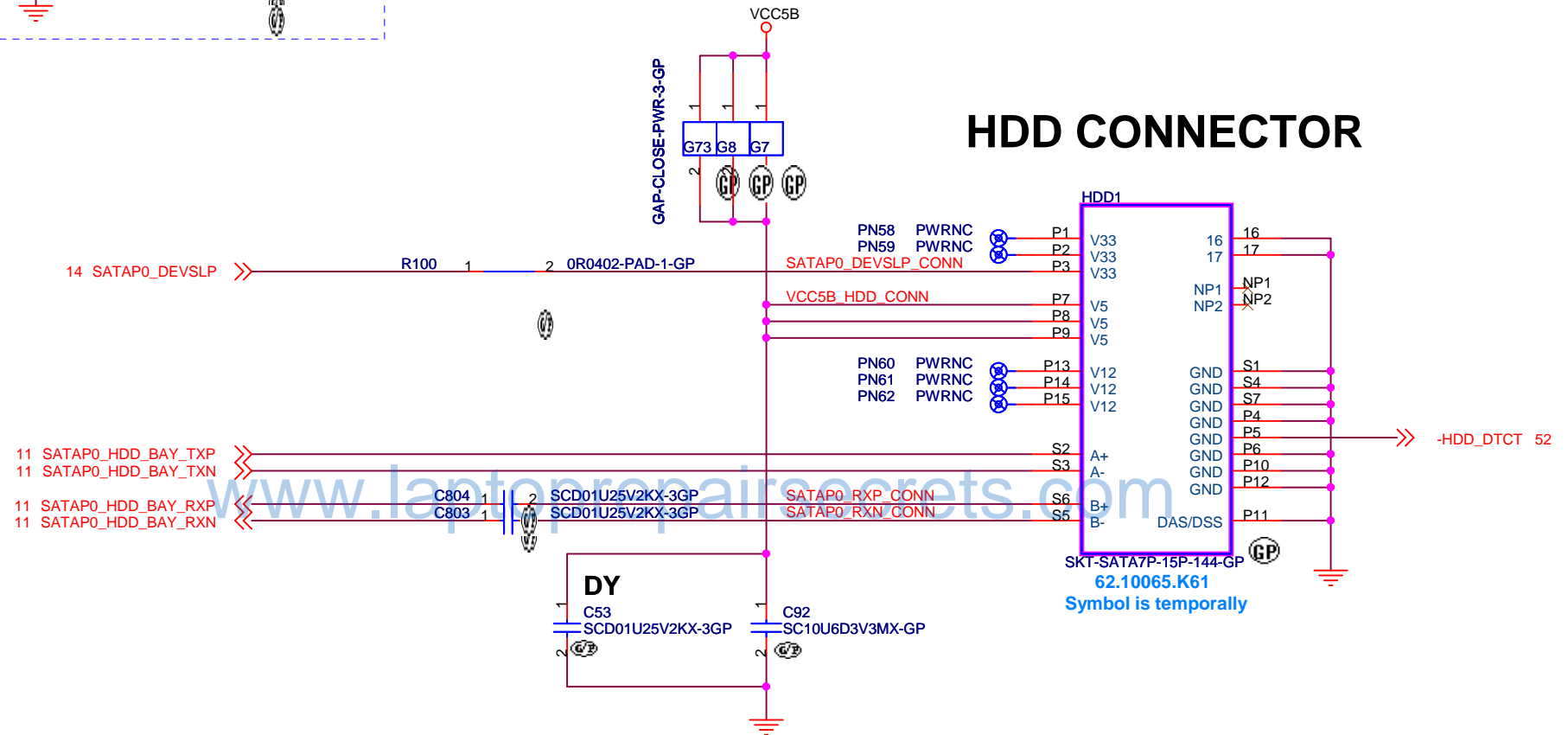
THUNDERBOLT CONNECTOR WS			
Size	Document Number	Rev	
A2	Kome-1 WS	-1	
Date	Thursday, September 12, 2013	Sheet	37 of 106



## Near SATA HDD CONN: HDD1 (p.039)



## HDD CONNECTOR



<Variant Name>

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**SATA HDD I/F**

Size  
A4

Document Number

**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

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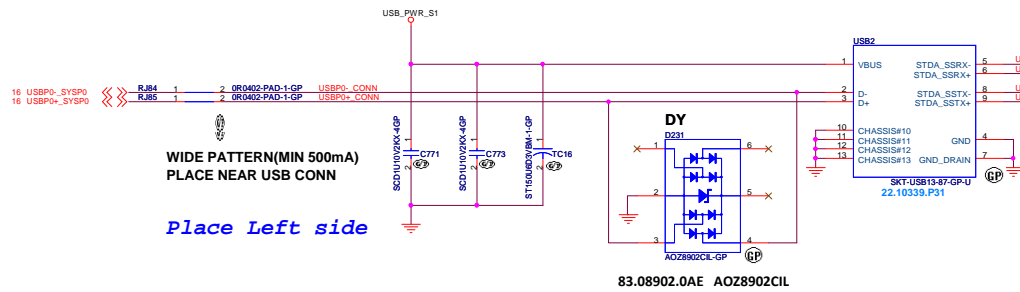
www.laptoprepairssecrets.com

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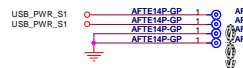
<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserve for ODD IF Con		
Size	Document Number	Rev
A4	Kome-1 WS	-1
Date:	Wednesday, July 17, 2013	Sheet 40 of 105

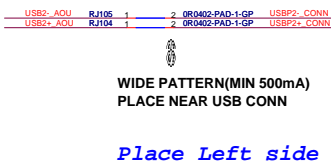
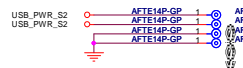




Near USB3.0 CONN: USB2 (p.041)



Near USB2.0 CONN: USB1 (p.041)



83.08902.0AE A0Z8902CIL

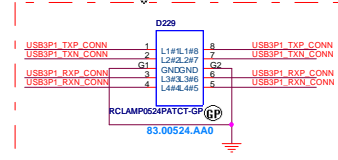
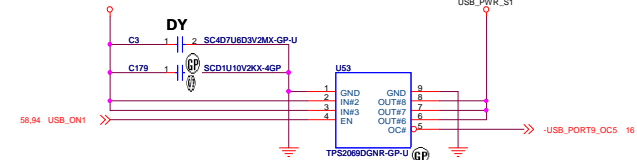


TABLE of TVS DIODE: D229

	Vendor	Vendor P/N	Wistron P/N
1st	SEMTECH	RClamp0524PATCT	83.00524.AA0
2nd	Littelfuse	SP3012-04UTG	83.03012.0A0
3rd	Infineon	ESD3V3U4ULC	83.3V3U4.0A0
4th	NXP	IP4294CZ10-TBR	83.04294.0A0

VCC5M\_IO\_PWR-



74.02069.079 TPS2069 without discharge function  
74.02069.A79 TPS2069C with discharge function

FOR ON BOARD SINGLE USB 3.0 CONNECTOR  
Continuous Current Limit 1.5A

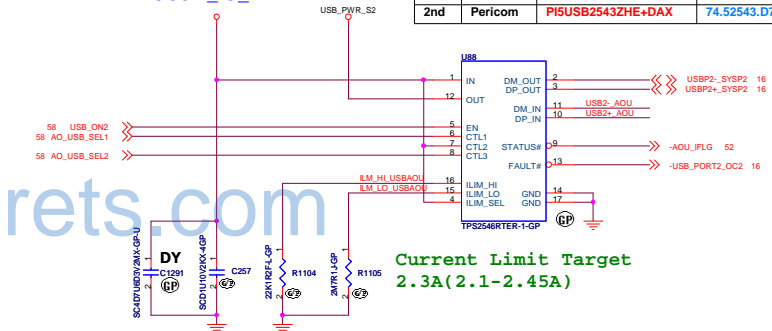
TABLE of USB 3.0 port: U53

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069DGN	74.02069.079
2nd	GMT	G548A1F51U	74.00548.A79

TABLE of AOU port: U88

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2546RTER (PG 1.1)	74.02546.A73
2nd	Pericom	PI5USB2543ZHE+DAX	74.52543.D73

VCC5M\_IO\_PWR-



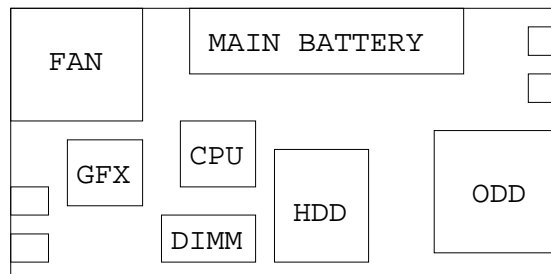
Current Limit Target  
2.3A(2.1-2.45A)

USB System Port Assignment List

Location	USB 2.0				USB 3.0	
	System Port	PCH Port	Signal Name	AOU Support	PCH Port	Signal Name
Left	Port 0	Port 0	USBP0_SYSP0	No	Port 1	USB3P1_SYSP0
Right	Port 1	Port 1	USBP1_SYSP1	No	Port 2	USB3P2_SYSP1
Left	Port 2	Port 2	USBP2_SYSP2	Yes		
Right	Port 3	Port 9	USBP9_SYSP3	No		

USB 2.0 Port 2 with AOU

USB 3.0 Port 1  
USB 2.0 Port 0



USB 2.0 Port 9

USB 3.0 Port 2  
USB 2.0 Port 1

<Variant Name>

緯創資通 Wistron Corporation	
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsichuan, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Size	
A2	
Document Number	
Kome-1 WS	
Date: Thursday, September 12, 2013	
Sheet 41 of 106	
Rev -1	



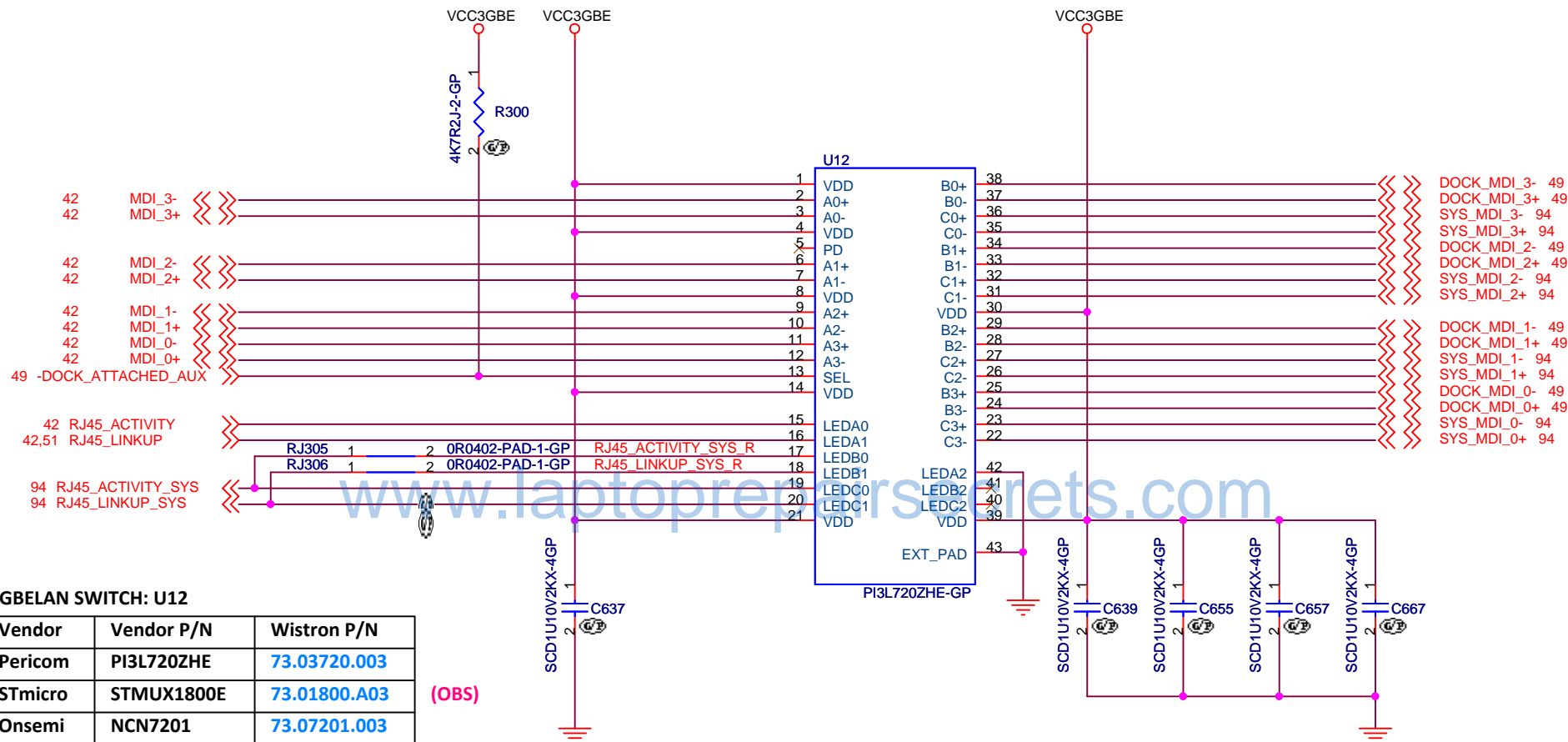



TABLE of GBELAN SWITCH: U12

	Vendor	Vendor P/N	Wistron P/N
1st	Pericom	PI3L720ZHE	73.03720.003
2nd	STmicro	STMUX1800E	73.01800.A03
3rd	Onsemi	NCN7201	73.07201.003

(OBS)

73.01800.A03 OBS REASON:  
Due to Broadcom LAN test fail with quality issue (lock on 2012.06.15)

<Variant Name>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>GBE LAN Switch</b>	
Size A4	Document Number <b>Kome-1 WS</b>
Date: Thursday, September 12, 2013	
Sheet 43 of 105	

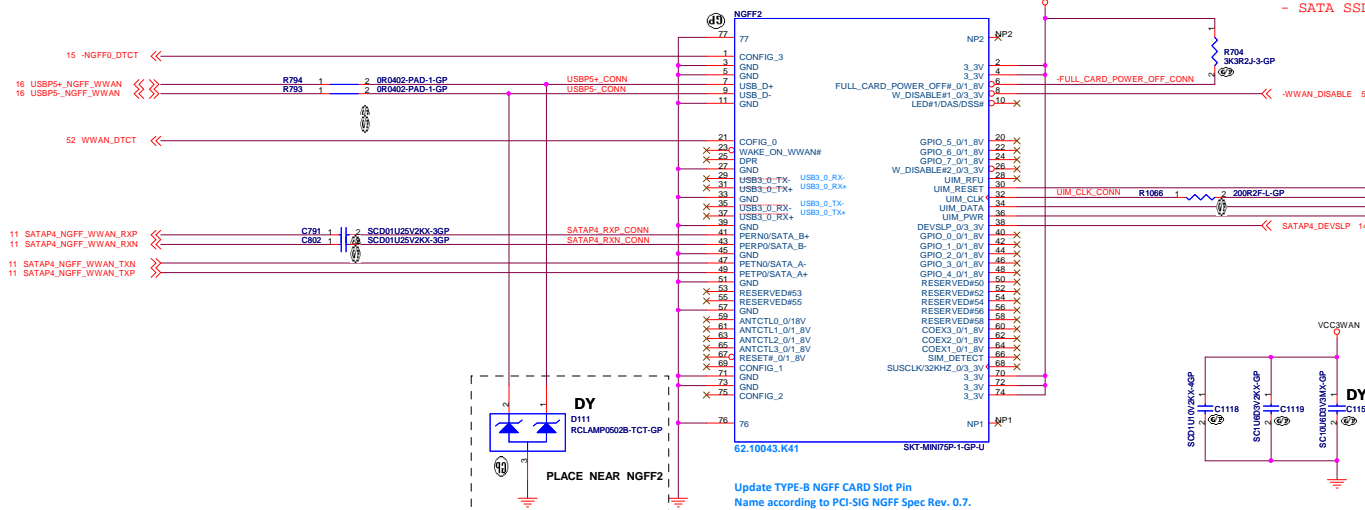
# TYPE-B (Socket2) NGFF CARD FOR WWAN/SSD

3.2H CONNECTOR

This Card slot supports  
- USB 2.0 based WWAN interface  
with SSIC based Port 0 config  
- SATA SSD Interface

## Near SIM CONN: SIM1 (p.044)

UIM RESET	AFT14P-GP	1	AFTP36
UIM CLK	AFT14P-GP	2	AFTP36
UIM DATA	AFT14P-GP	3	AFTP37
UIM PWR	AFT14P-GP	4	AFTP38

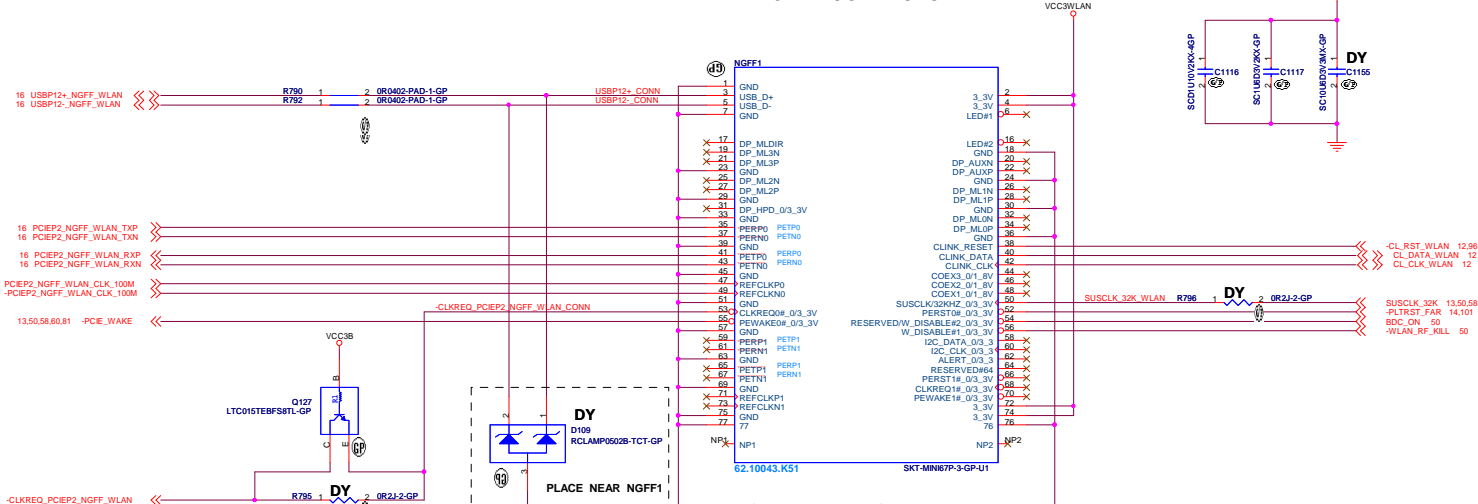


83.00502.AA1: (D109, D111)  
OBS REASON: For contract issue,  
replaced by 75.00502.07D

NGFF WWAN/SSD Slot		NGFF SSD Slot	
	-NGFF0_DTCT	WWAN_DTCT	-MSATA_DTCT
WWAN	Low	High	N/A
SSD	Low	Low	Low
No Card	High	High	High
Reserved	High	Low	High
Reserved			Low

# TYPE-A NGFF CARD FOR WLAN

3.2H CONNECTOR



83.00502.AA1: (D109, D111)  
OBS REASON: For contract issue,  
replaced by 75.00502.07D

<Variant Name>

緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsueh,  
Taipei Hsien 221, Taiwan, R.O.C.

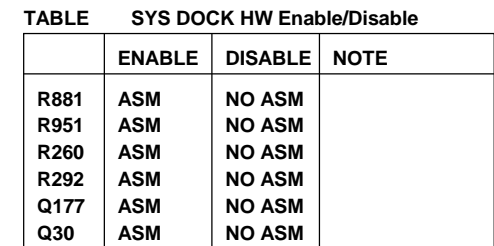
File NGFF Slot x 2  
Size A2 Document Number Kome-1 WS  
Date: Thursday, September 12, 2013 Sheet 44 of 106



N78826754  
 HP\_L\_JACK\_C  
 HP\_R\_JACK\_C  
 HP\_JACK\_SYS  
 47 MIC\_RING2  
 47 MIC\_SLEEVE

AFTE14P-GP 1  
 AFTE14P-GP 2  
 AFTE14P-GP 3  
 AFTE14P-GP 4  
 AFTE14P-GP 5  
 AFTE14P-GP 1  
 AFTE14P-GP 1  
 AFTE14P-GP 1

AFTP42  
 AFTP43  
 AFTP44  
 AFTP45  
 AFTP46  
 AFTP47  
 AFTP48

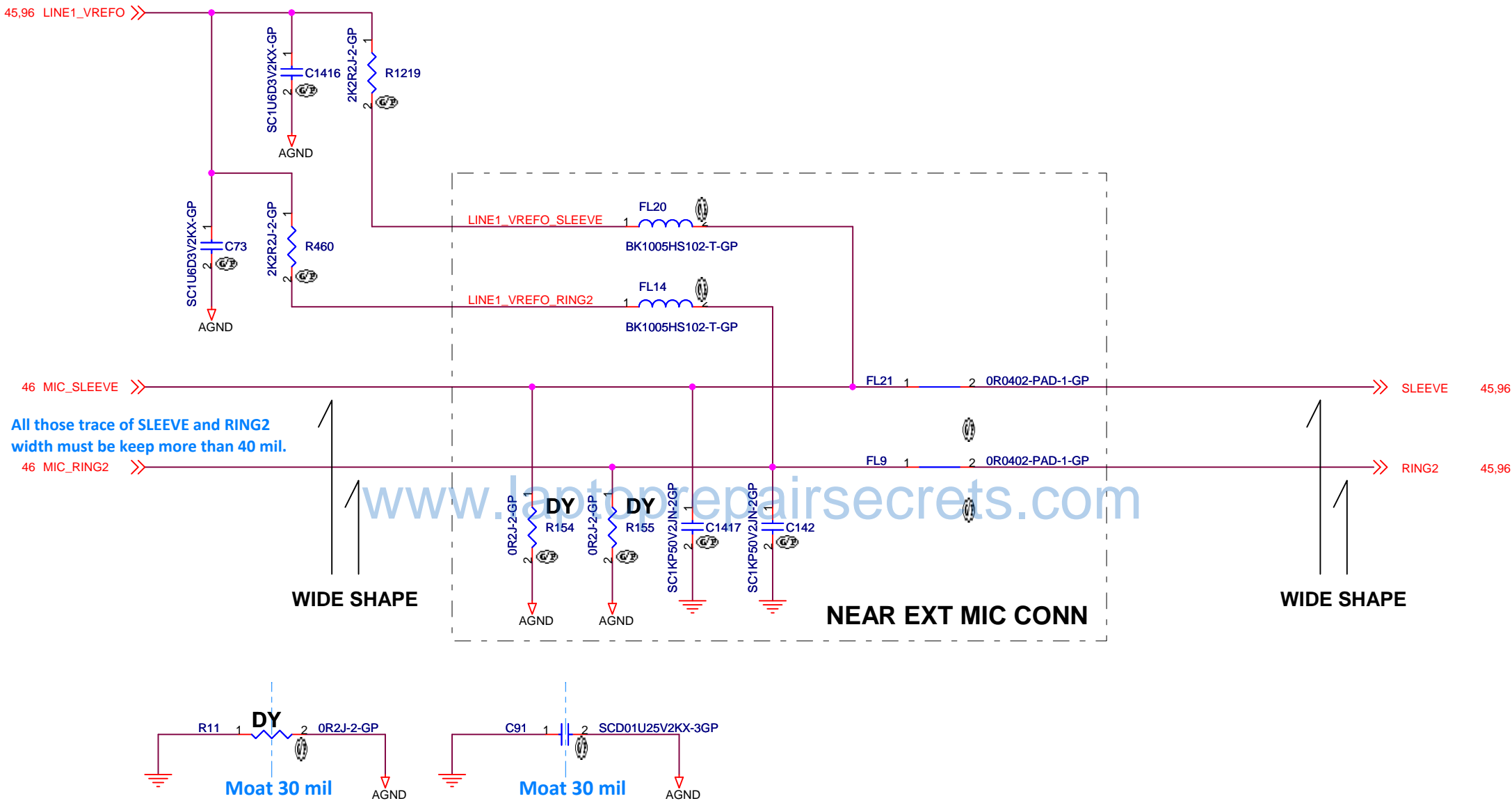


LOGIC

<Variant Name>

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>Audio Headset Jack</b>			
Size	Document Number	Rev	
A3	<b>Kome-1 WS</b>	<b>-1</b>	
Date:	Thursday, September 12, 2013	Sheet	46 of 105



<Variant Name>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Audio EXT MIC I/F**

Size  
A4

Document Number

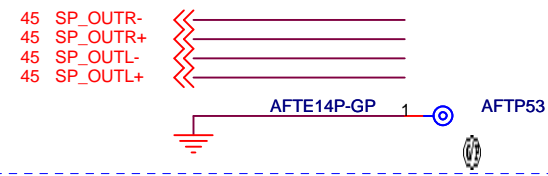
**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

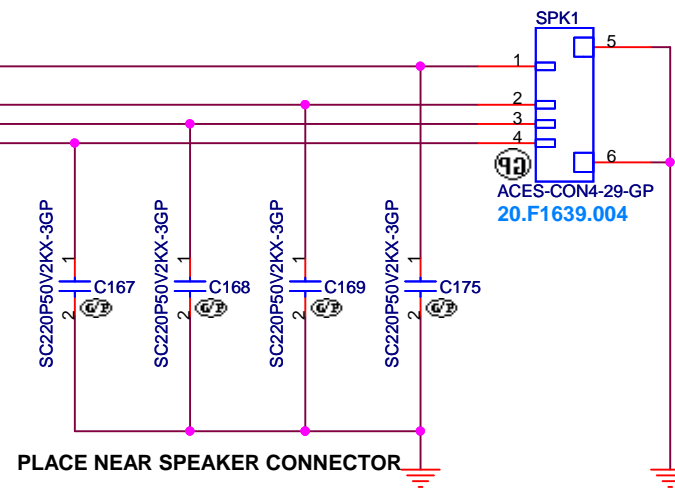
Sheet 47 of 105

Near SPEAKER CONN: SPK1 (p.048)

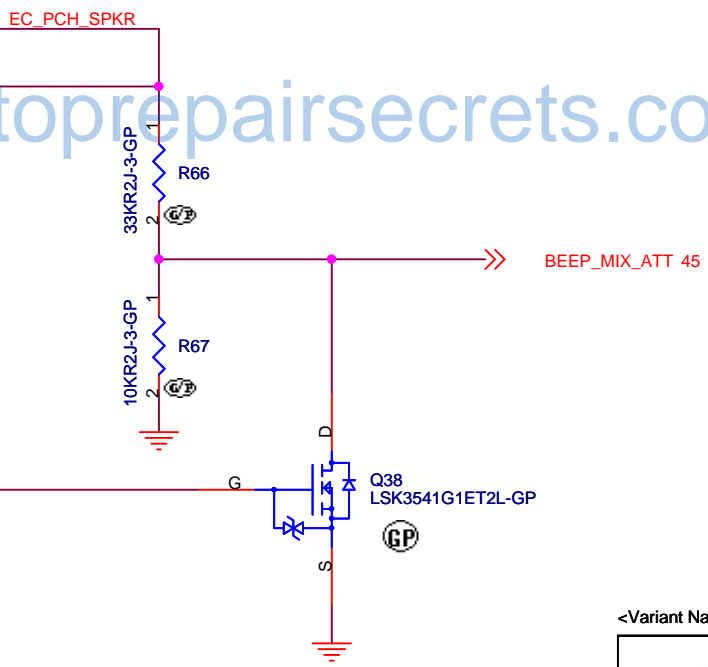
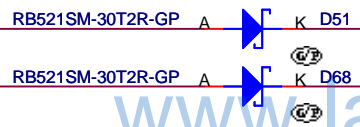


Delete AFTP49, AFTP50, AFTP51, AFTP52 for layout placement

45 SP\_OUTL+  
45 SP\_OUTL-  
45 SP\_OUTR-  
45 SP\_OUTR+



50 EC\_SPKR  
11 PCH\_SPKR

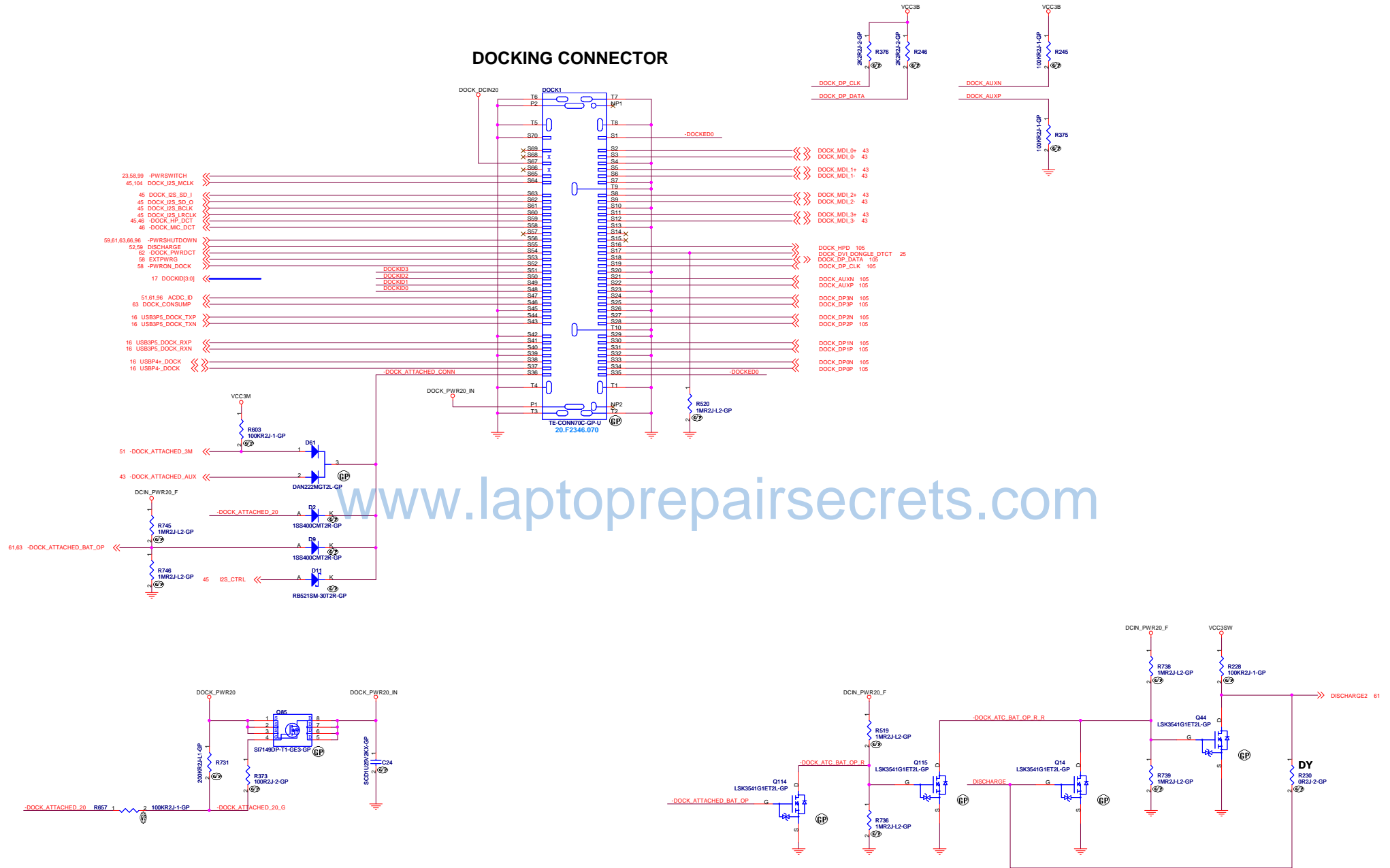


<Variant Name>

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AUDIO SPEAKER I/F , BEEP			
Size A4	Document Number  Kome-1 WS		Rev  -1
Date: Thursday, September 12, 2013		Sheet 48	of 105



# DOCKING CONNECTOR

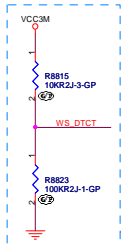
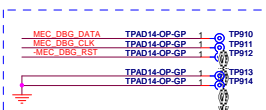






WS_DTCT (GPIO105)		
R8815	UMA/SWG	WS
	NO_ASM	ASM

LOGIC



Graphics Matrix					
GPIO172 (VIDEO_ID)	UMA Entry	UMA Enhance	SWG	WS NVIDIA	WS AMD
GPIO172 (VIDEO_ID)	L	L	H	H	L
GPIO105 (WS_DTCT)	L	L	L	H	H

JTAG debug port		
	Enable	Disable
R8796	ASM	NO_ASM
R8797	NO_ASM	ASM

LOGIC

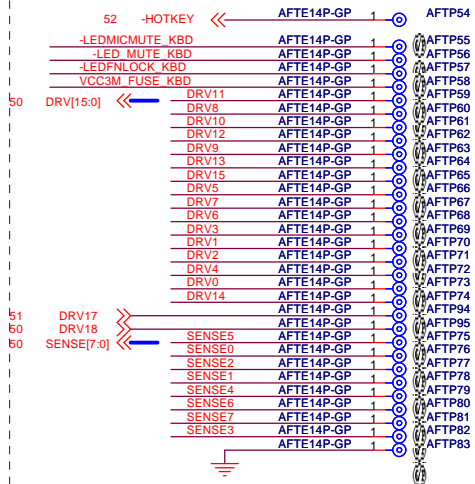
Trace FIFO debug port		
	Enable	Disable
R8807	ASM	NO_ASM
R8808	NO_ASM	NO_ASM
R8950	NO_ASM	ASM

LOGIC

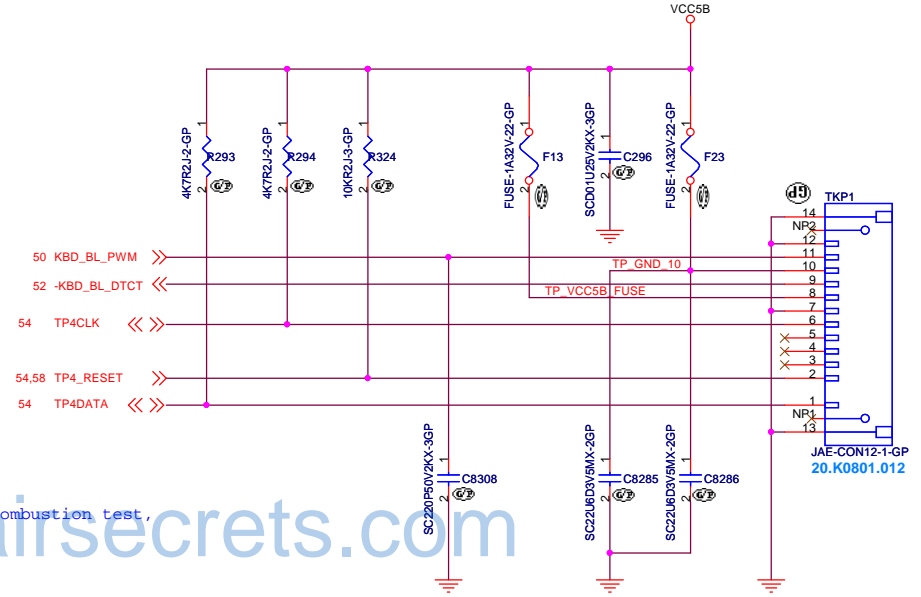
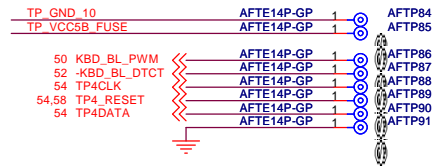
VIDEO ID (GPIO172)			
	UMA/AMD WS	SWG/nVIDIA WS	
R940	NO_ASM	ASM	

LOGIC

## Near Keyboard CONN: KBD1 (p.053)



## Near TrackPoint CONN: TKP1 (p.053)



**CLOSE-GAP**  
If we will face the failure on combustion test,  
Need to replace to 0.5A Fuse.

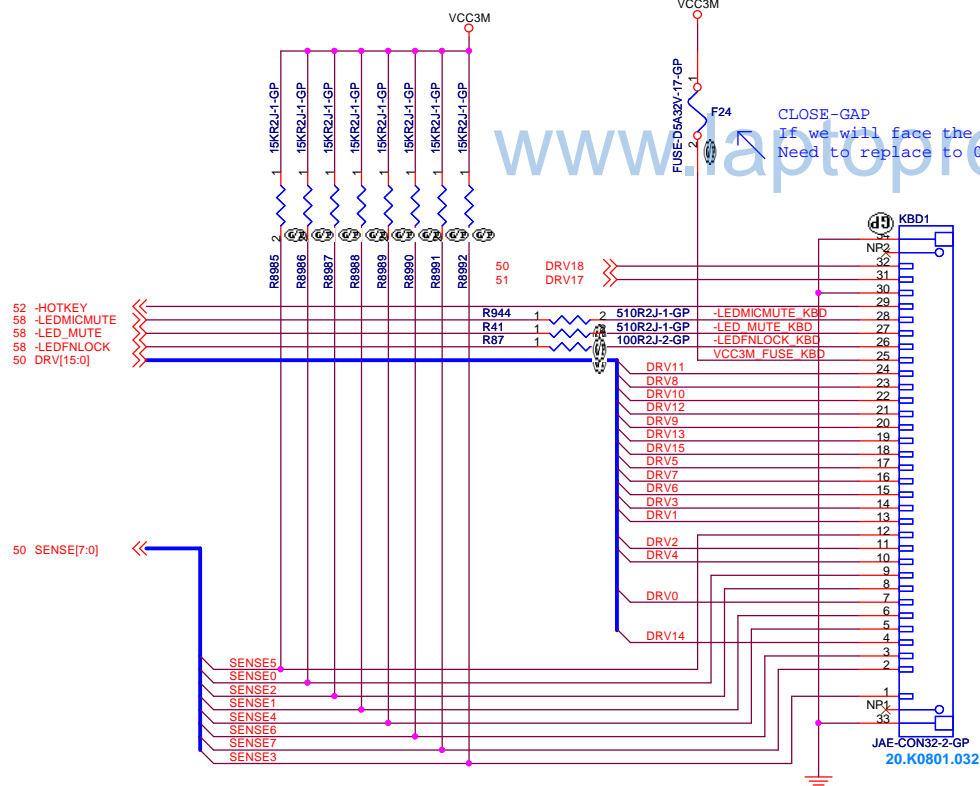
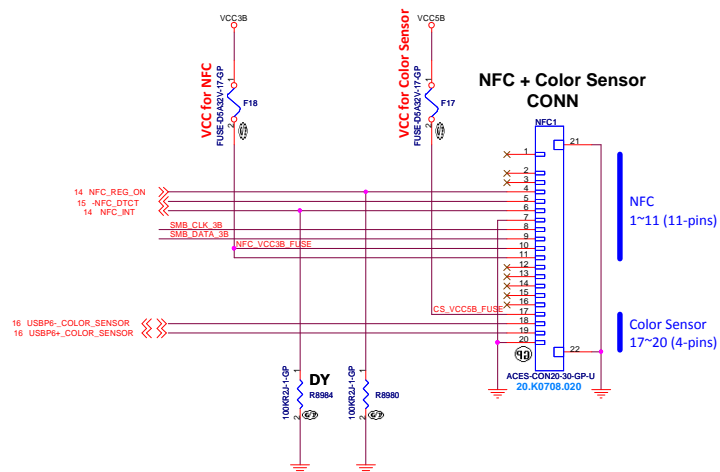


Diagram showing the connections for pins 1 through 5 of the AFT100 module:

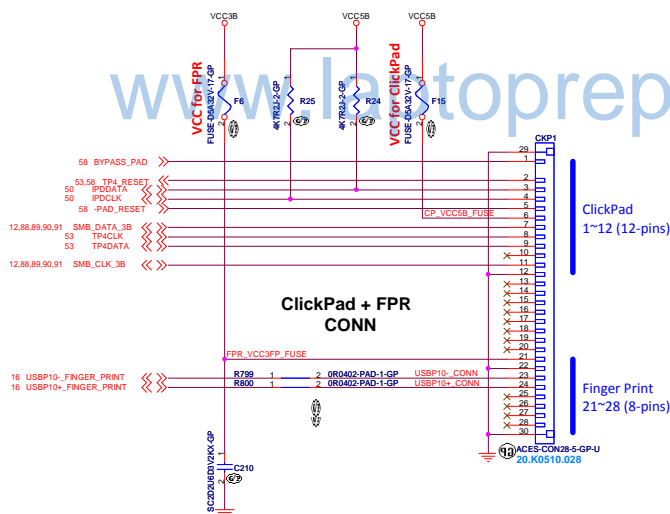
- Pin 1: NFC\_VCC3B\_FUSE to AFT14P-GP
- Pin 2: 14 NFC\_INT to AFT14P-GP
- Pin 3: 15 NFC\_DTCT to AFT14P-GP
- Pin 4: 14 NFC\_REG\_ON to AFT14P-GP
- Pin 5: CS\_VCC5B\_FUSE to AFT14P-GP

The AFT100 module is shown with pins 1 through 5 connected to the AFT14P-GP pins. The AFT100 module is labeled AFT100, AFTP101, AFTP111, AFTP112, AFTP93, and AFTP98.



	UNIT NO.	Wistron P/N	PIN NO.	DESCRIPTION	CABLE TYPE
Before	FPR1	20.K0793.012	12	FPR+COLOR SENSOR	FPC
After	NFC1	20.K0708.020	20	COLOR SENSOR+NFC	FFC
Before	CKP1	20.K0767.026	26	CLICK PAD+NFC	FFC
After	CKP1	20.K0510.028	28	FPR+CLICK PAD	FFC

FPR_VCC5P_FUSE	AFTE14P_FUSE	AFPT92
CP_VCC5P_FUSE		AFPT99
53.58 TP4_RESET	AFTE14P_FUSE 1	AFPT102
53 TP4DATA	AFTE14P_FUSE 1	AFPT103
53 TP4CLK	AFTE14P_FUSE 1	AFPT104
12.88.89.90.91 SMB_DATA_3B	AFTE14P_FUSE 1	AFPT105
12.88.89.90.91 SMB_CLK_3B	AFTE14P_FUSE 1	AFPT106
58 BYPASS_PAD	AFTE14P_FUSE 1	AFPT107
58 PAD_RESET	AFTE14P_FUSE 1	AFPT108
50 P0CLK	AFTE14P_FUSE 1	AFPT109
50 P0DATA	AFTE14P_FUSE 1	AFPT110
	AFTE14P_FUSE 1	AFPT113

[illegible][illegible]

Pin Order

6	GND (DTCT#)
5	NC
4	GND
3	USB DN
2	USB DP
1	VCC5B



SmartCard

6 DTCT#

5 NC

4 GND

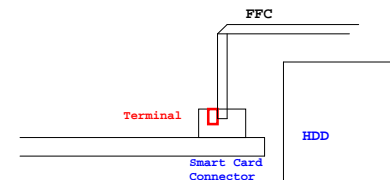
3 USB DN

2 USB DP

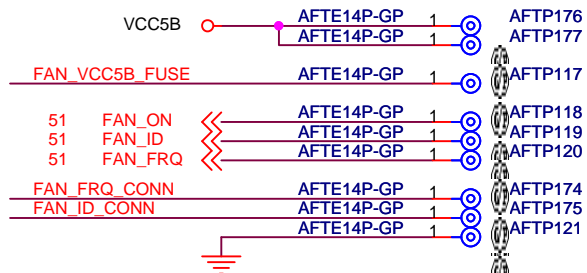
1 VCCSB

SmartCard

Connector is placed on bottom side.



## Near FAN CONN: FAN1/FAN3 (p.055)

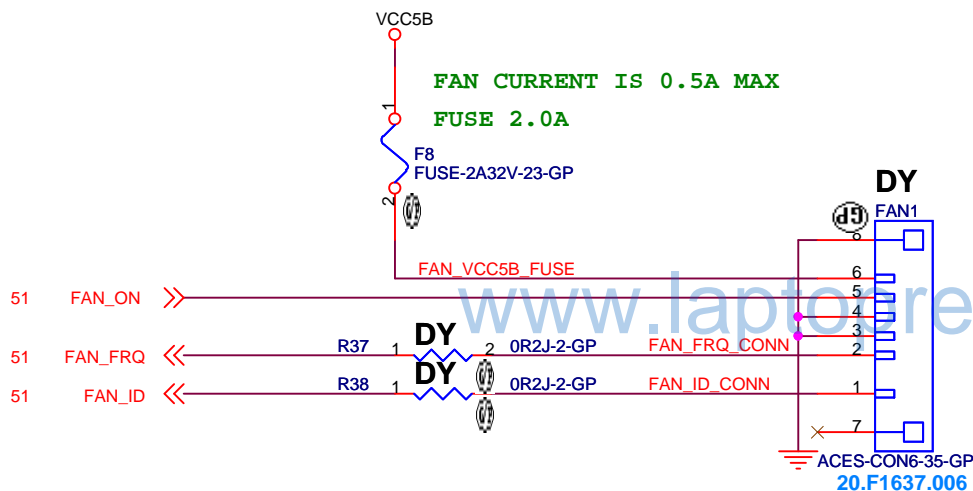


TOP Side  
Bottom Side

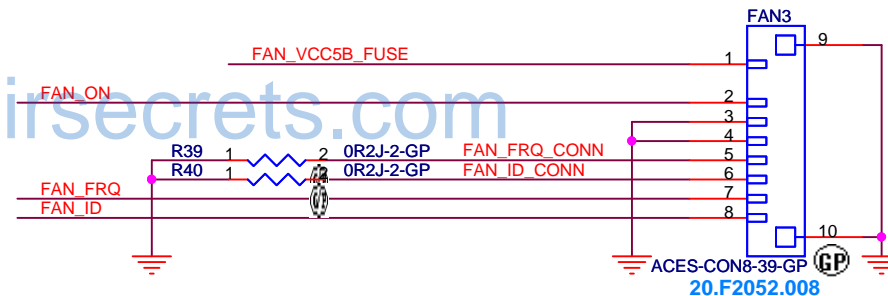
As Space from Metal heat Plate to top of  
GFX die is different on Q3 model and Q1 model,  
FAN module should be different.

FAN Module	Pin No.	FAN3	FAN1
For Q1 GFX	8	<b>ASM</b>	<b>NO_ASM</b>
For Q3 GFX	6	<b>NO_ASM</b>	<b>ASM</b>

↑  
LOGIC



FAN1 co-lay with FAN3



FAN ID is defined with analog level.

<Variant Name>

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Title

**FAN I/F**

Size  
A4

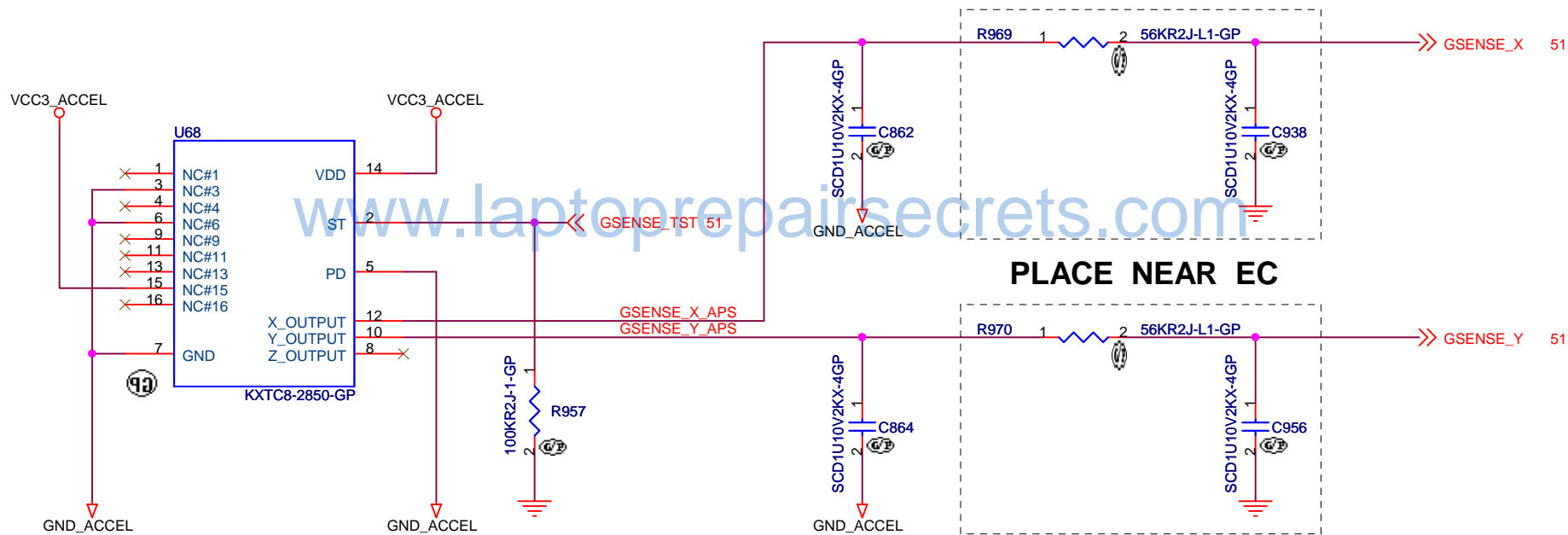
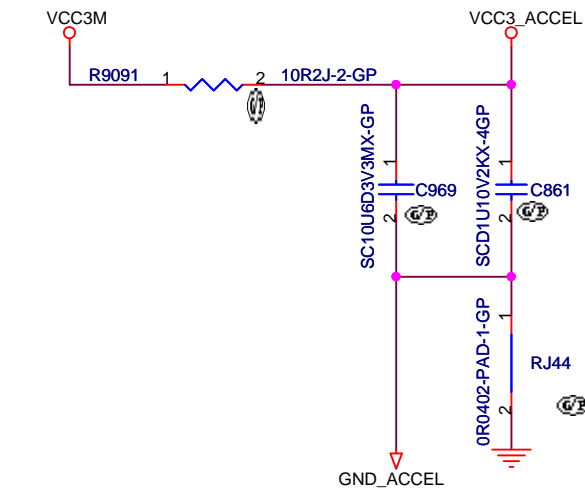
Document Number

**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

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These components must be placed near HDD and same location for UMA/SWG/WS.

Do not use Z-axis monitor on APS

<Variant Name>

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Title

**APS(G SENSOR)**

Size  
A4

Document Number

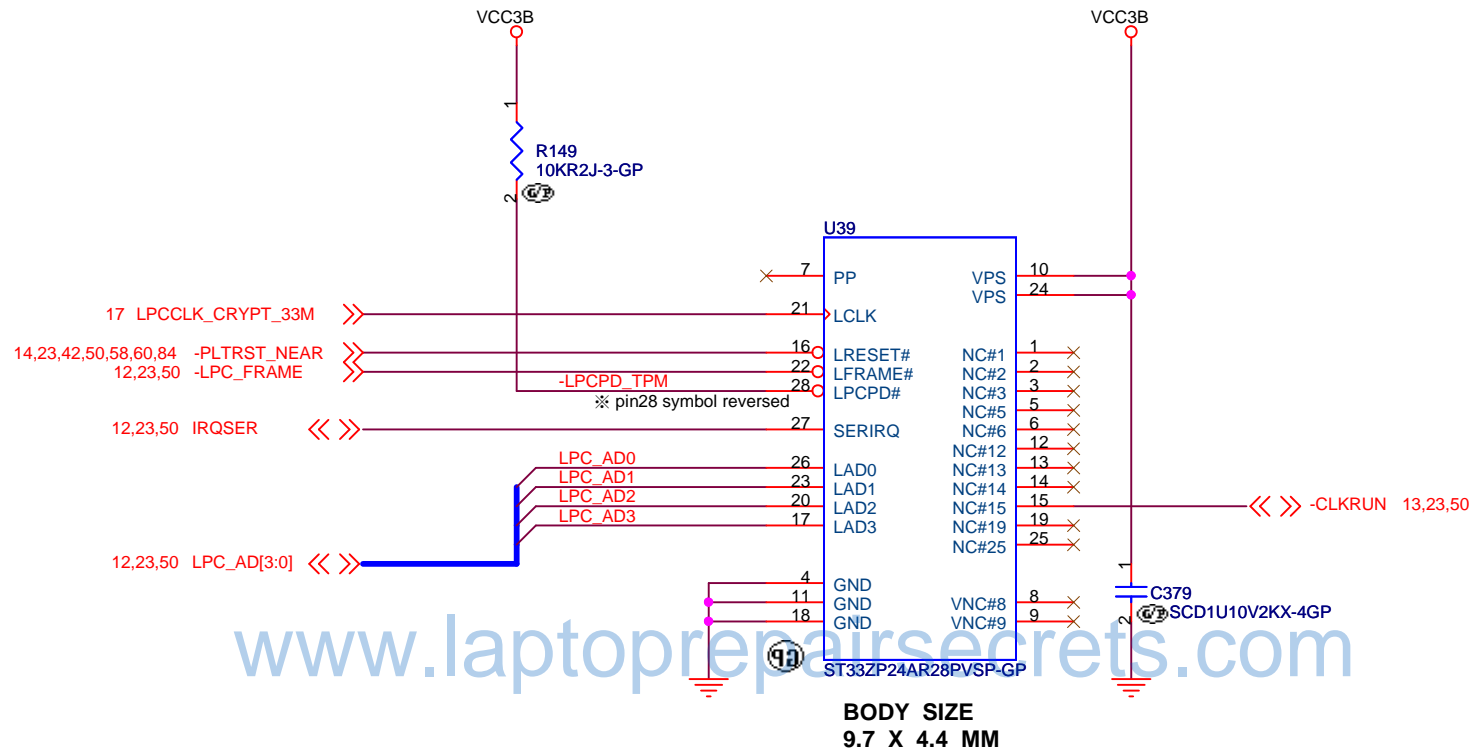
**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

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Need to update the firmware to improve system boot up time.

<Variant Name>

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Title

**TPM**

Size  
A4

Document Number

**Kome-1 WS**

Rev  
-1

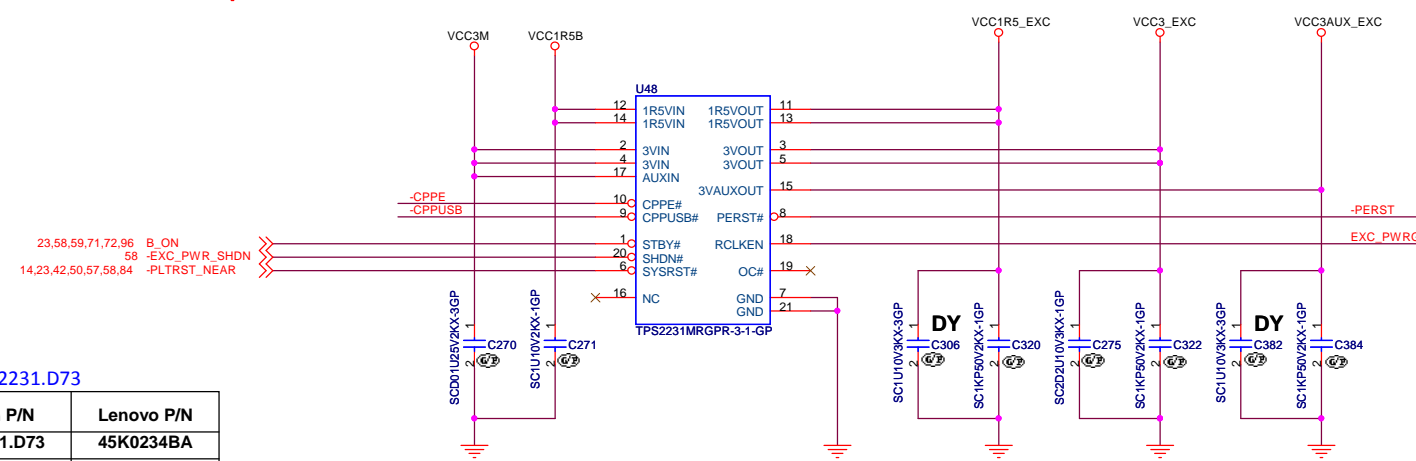
Date: Thursday, September 12, 2013

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Signal	AFTE14P-GP Pin	AFPT Pin
VCC1R5_EXC	1	AFPT122
VCC3AUX_EXC	2	AFPT123
VCC3_EXC	3	AFPT124
-CPUSS	4	AFPT125
EXP_CONN 7	5	AFPT126
EXP_CONN 8	6	AFPT127
-PERST	7	AFPT128
EXC_PWRG_CONN	8	AFPT129
-CPPE	9	AFPT130
PCIE_WAKE	10	AFPT131
		AFPT132

[illegible]

	Supplier	Vendor P/N	Wistron P/N	Lenovo P/N
U48	TI	TPS2231MRGPR-3	74.02231.D73	45K0234BA
	NUVOTON	W83L351YG V.ASA	74.83351.A73	
	ROHM	BD4157MUV-GE2	74.04157.A73	
	ROHM	BD4156MUV-SGE2	74.04156.A73	

DCIN\_PWR20\_F\_CONN

ACDC\_ID\_CONN

AFTE14P-GP

AFTE14P-GP

AFTE14P-GP

AFTE14P-GP

AFTE14P-GP

AFTE14P-GP

AFTE14P-GP

AFTP133

AFTP134

AFTP135

AFTP136

AFTP137

AFTP138

AFTP139



PEAK SHIFT	YES	NO
R662	NO-ASM	ASM
R369	ASM	NO-ASM
Q78	ASM	NO-ASM
Q51	ASM	NO-ASM

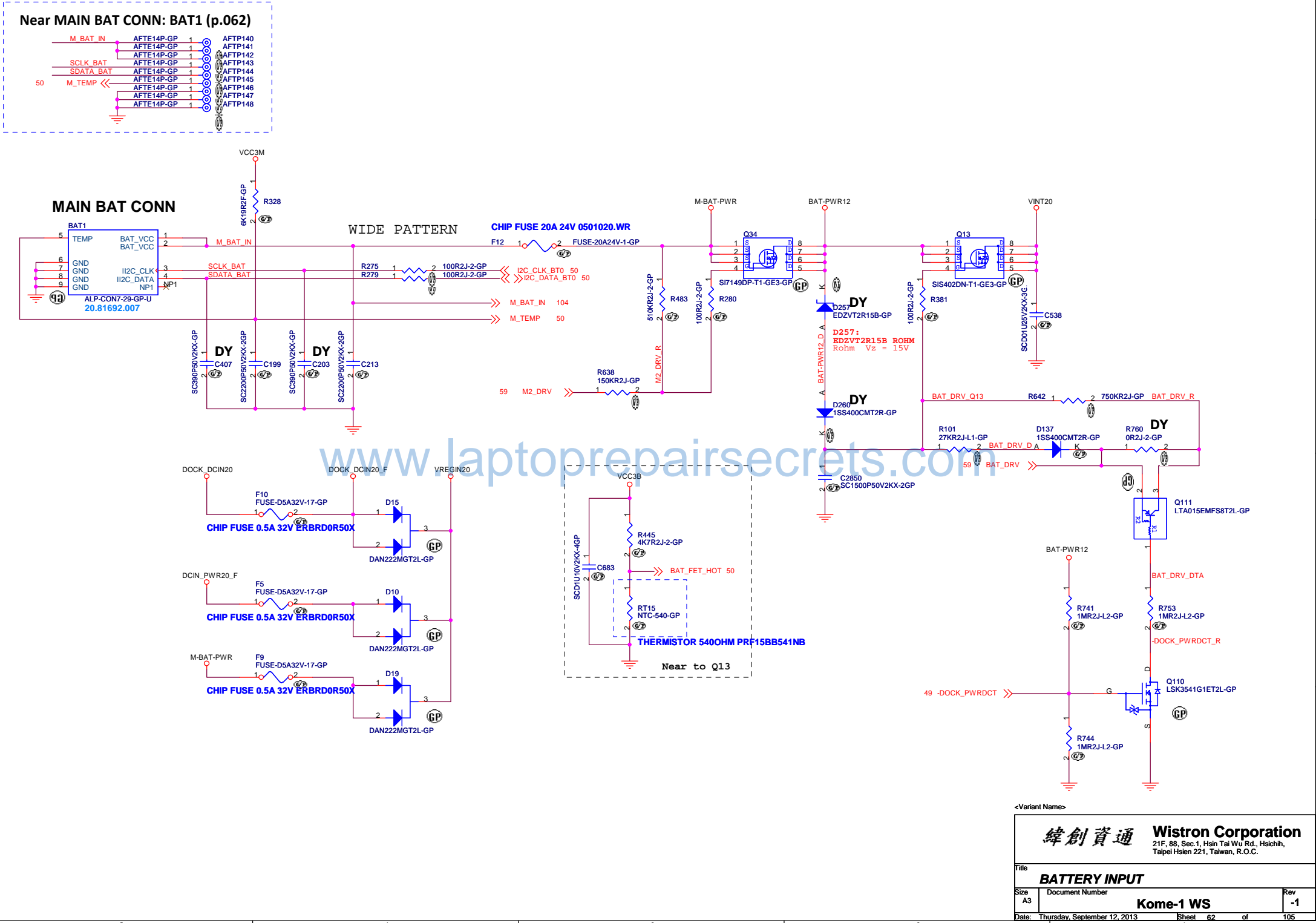
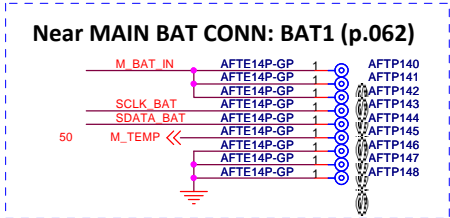
<Variant Name>

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Title <b>DC IN</b>			
Size A2	Document Number <b>Kome-1 WS</b>	Rev <b>-1</b>	
Date: <b>Thursday, September 12 2013</b>		Sheet <b>61</b>	of <b>105</b>

**Near MAIN BAT CONN: BAT1 (p.062)**

Signal	Pin	Signal	Pin
M_BAT_IN	1	AFTP140	10
	2	AFTP141	11
SCLK BAT	3	AFTP142	12
SDATA BAT	4	AFTP143	13
	5	AFTP144	14
M_TEMP	6	AFTP145	15
	7	AFTP146	16
	8	AFTP147	17
	9	AFTP148	18



<Variant Name>

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Title	
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### BATTERY INPUT

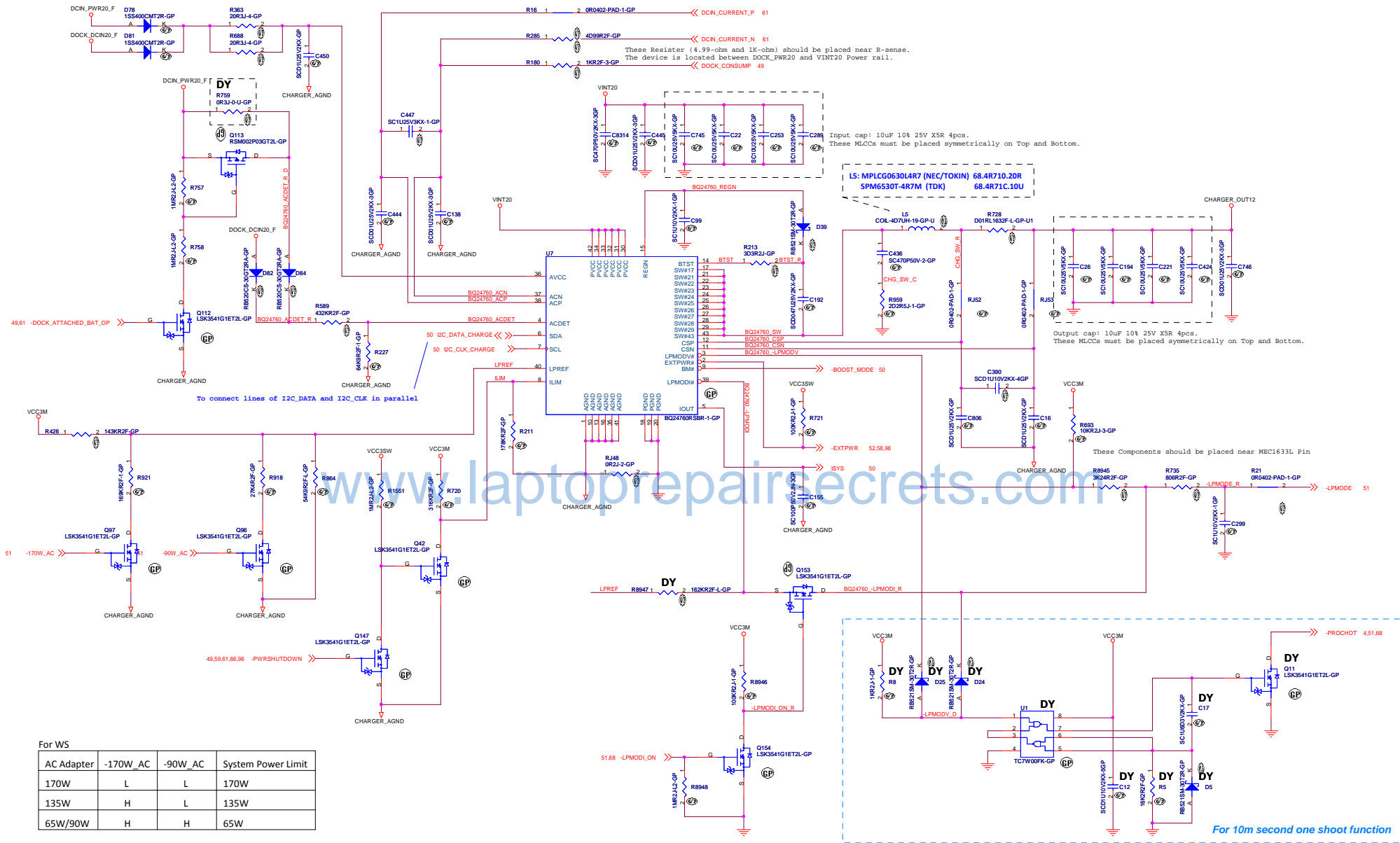
Size A3	Document Number <b>Kome-1 WS</b>	Rev -1
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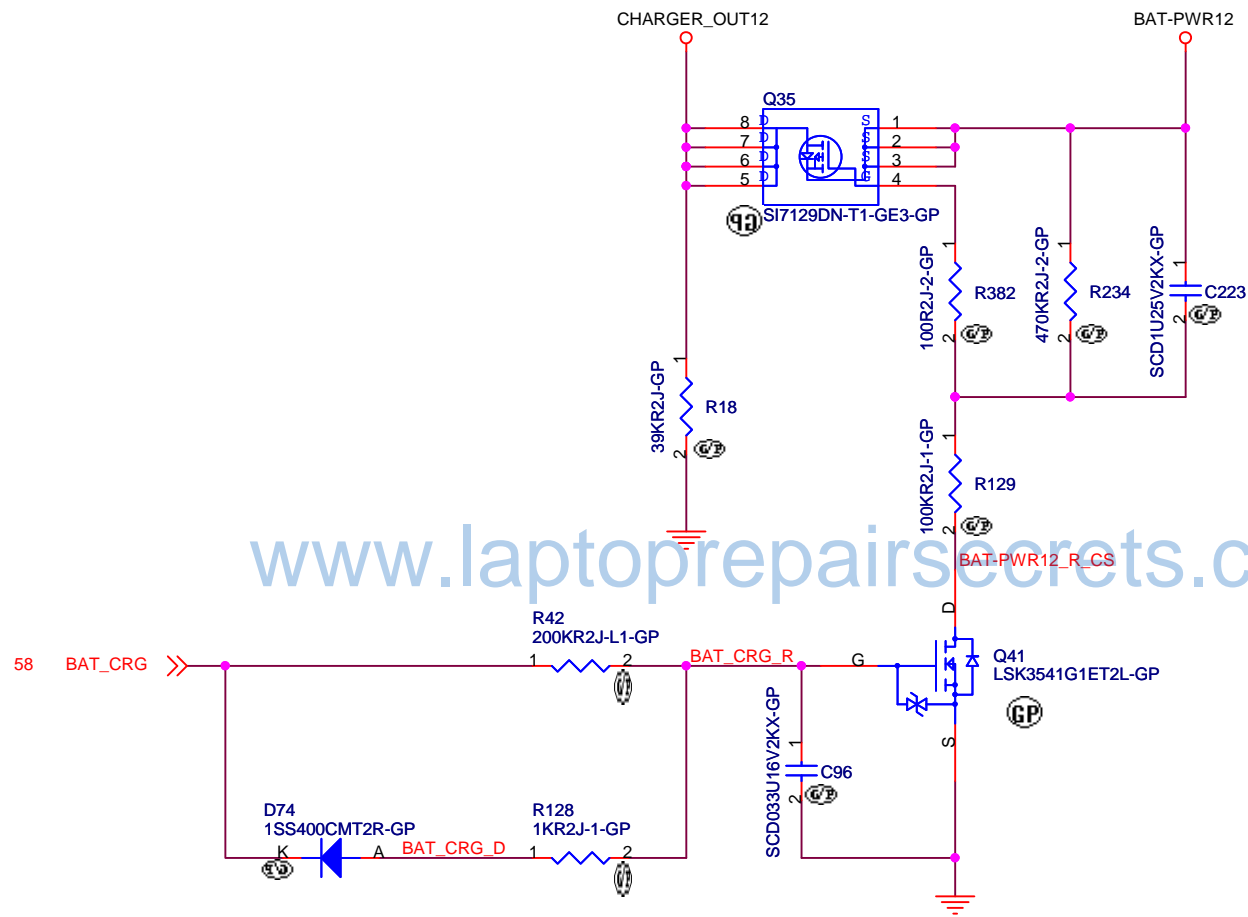
Size A3	Document Number <b>Kome-1 WS</b>	Rev <b>-1</b>
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Size A3	Document Number <b>Kome-1 WS</b>	Rev -1
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<Variant Name>

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Title

**CHARGER SELECT**

Size  
A4

Document Number

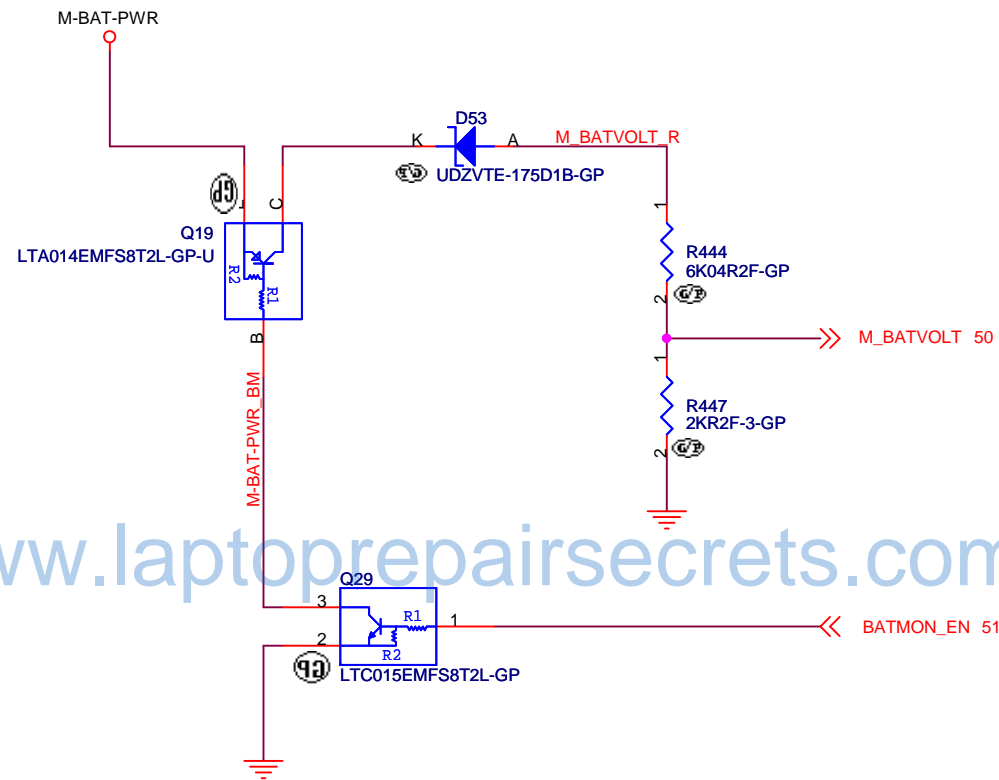
**Kome-1 WS**

Rev  
-1

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<Variant Name>

緯創資通

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Title

**BATTERY MONITOR**

Size  
A4

Document Number

**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

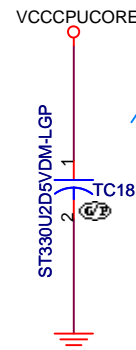
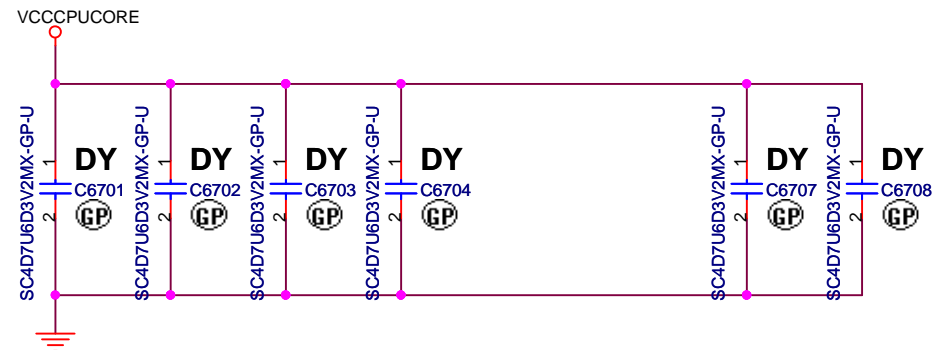
Sheet 65 of 105

Input cap : 10uF 10% 25V X5R 1206 6pcs  
These MLCCs must be placed symmetrically on Top and bottom.

Input cap : 10uF 10% 25V X5R 1206 6pcs  
These MLCCs must be placed symmetrically on Top and bottom.

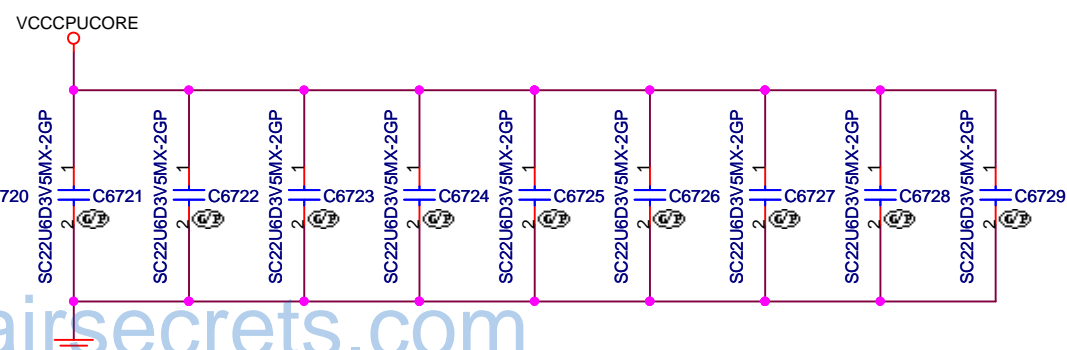
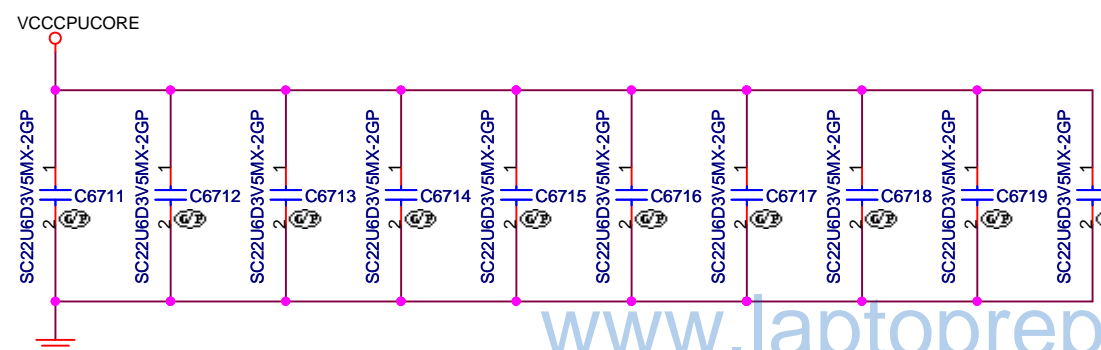


Title <b>VCC3M/5M</b>			
Size A2	Document Number <b>Kome-1 WS</b>		Rev <b>-1</b>
Date: <b>Thursday, September 12, 2013</b>		Sheet <b>66</b> of	<b>105</b>



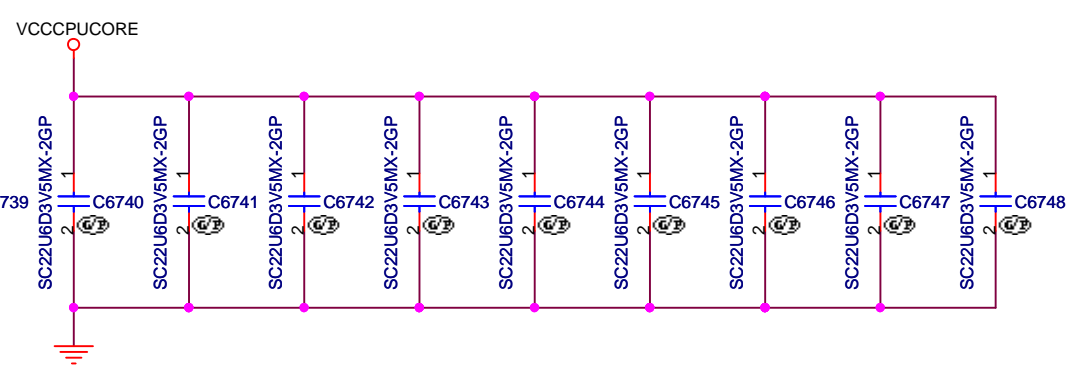
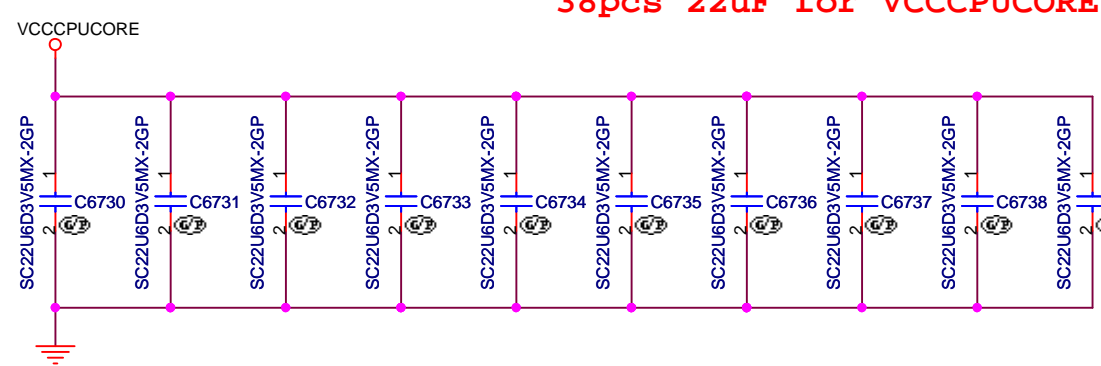
**TC18:**  
**For TPS51631 undershoot voltage issue**

TC18: 330uF 2.5V 9mOhm 7343-size  
 1st Kemet T520V337M2R5ATE009 80.3371V.L01  
 2nd Panasonic EEFSX0E331ER 077.53371.0001



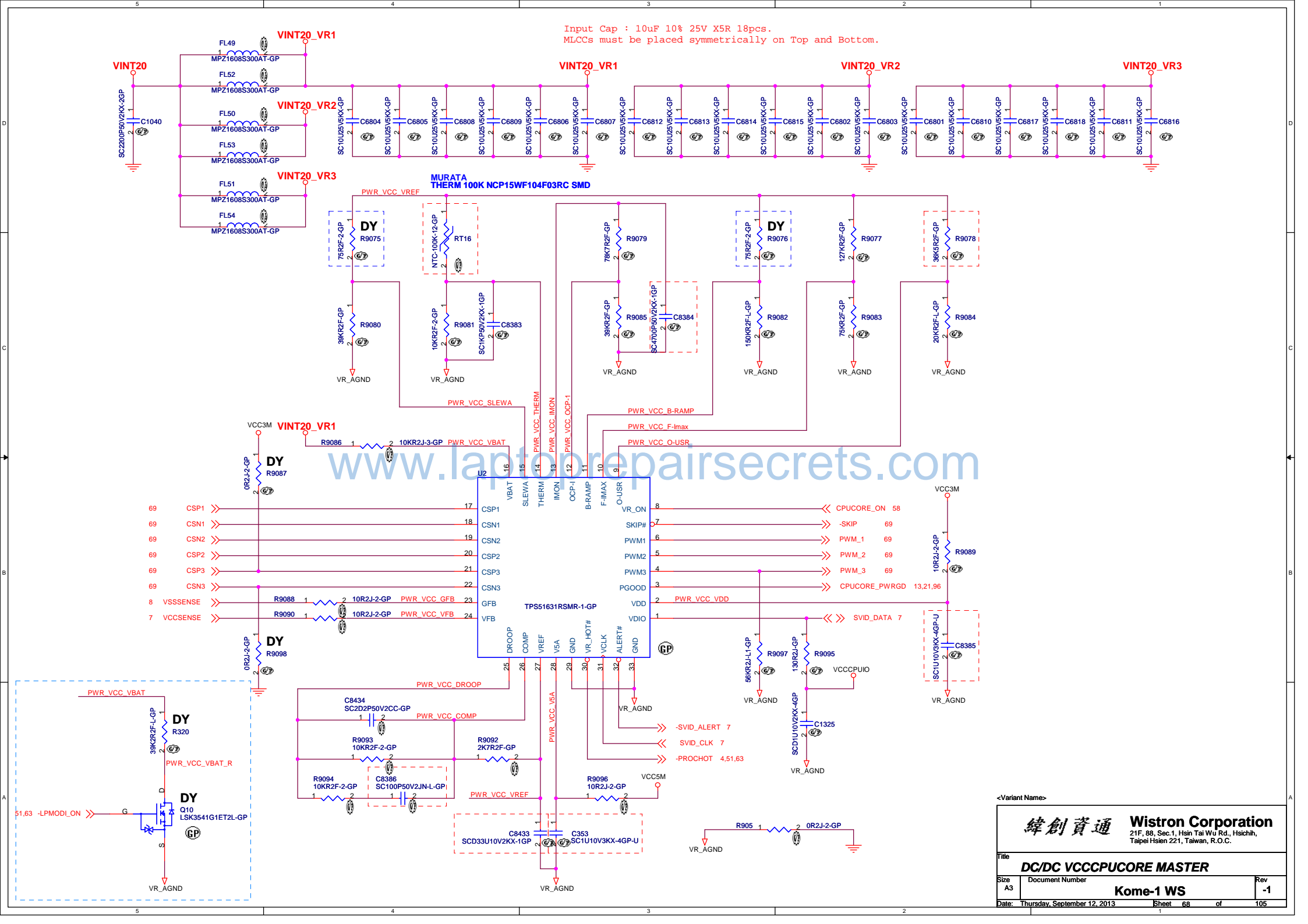
www.laptoprepairsecrets.com

38pcs 22uF for VCCCPUCORE

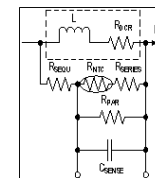
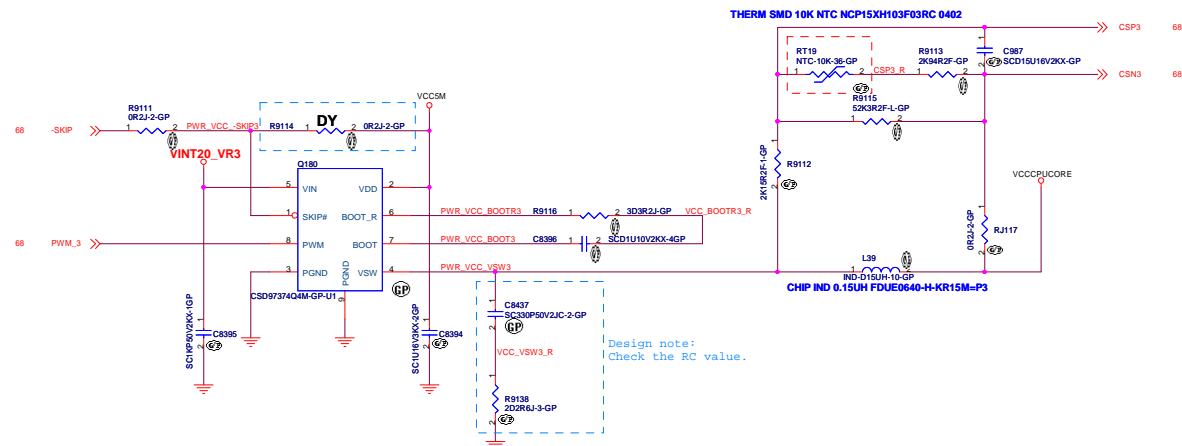
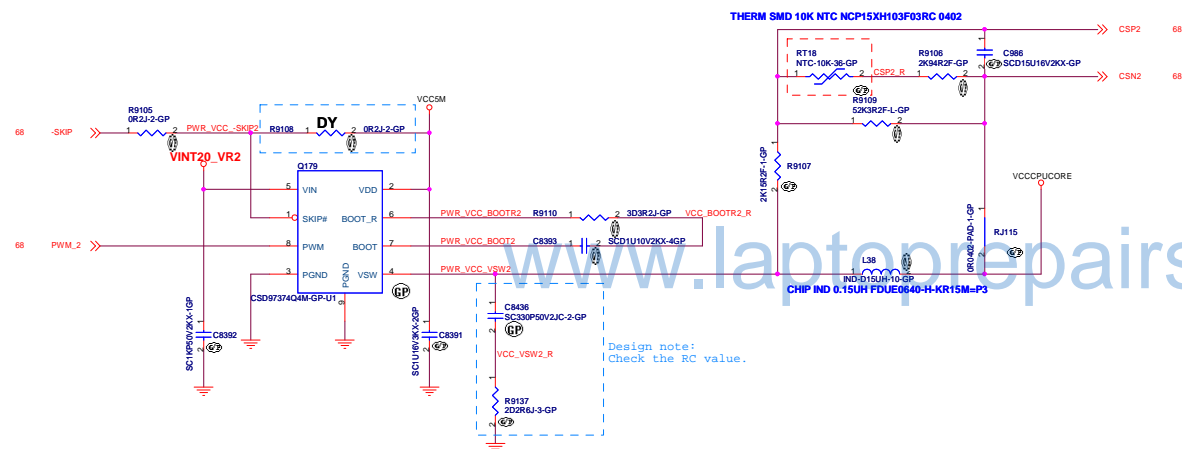
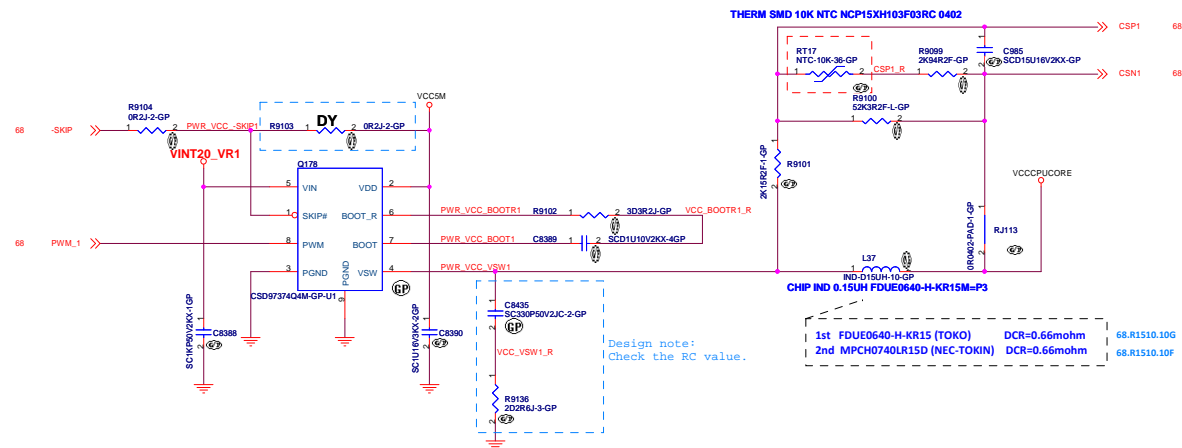


<Variant Name>

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>DC/DC VCCCPUCORE DECOUPLING</b>		
Title Size A4	Document Number <b>Kome-1 WS</b>	Rev <b>-1</b>
Date: Monday, July 22, 2013 Sheet 67 of 105		



Input Cap : 10uF 10% 25V X5R 18pcs.  
MLCCs must be placed symmetrically on Top and Bottom.



Vin (Max) 20V  
Inductor FDUE0640-H-KR15 (TOKO) DCR=0.66mOhm  
Output Capacitor 22uF x 38pcs  
Controller IC TP51631

Remove phase-3 power stage components and connect CSP3 to 3.3V and CSN3 to GND for 2-phase 37W Vcore.

Connection	Component Name	37W 2 Phase	47W 3 Phase	57W 3 Phase	Unit	
O-USR to GND	R9084	20	20	20	K-Ohm	
O-USR to VREF	R9078	64.9	36.5	36.5	K-Ohm	
F-IMAX to GND	R9083	150	75	75	K-Ohm	
F-IMAX to VREF	R9077	549	147	127	K-Ohm	
B-RAMP to GND	R9082	150	150	150	K-Ohm	
B-RAMP to VREF	R9076	Open	Open	Open	K-Ohm	
OCF-I to GND	R9085	39	39	39	K-Ohm	
IMON to OCF-I	R9079	162	88.7	78.7	K-Ohm	Different setting on NEC-TOKIN
THERM to GND	R9081	10	10	10	K-Ohm	
THERM to VREF	RT16	100	100	100	K-Ohm	NTC
SLEWA to GND	R9080	39	39	39	K-Ohm	
SLEWA to VREF	R9075	Open	Open	Open	K-Ohm	
DROOP to COMP	R9093	10	10	10	K-Ohm	
DROOP to COMP	C8434	2.2	2.2	2.2	pF	
DROOP to COMP	R9094 + C8386	10K + 330p	10K + 100p	10K + 100p		
COMP to VREF	R9092	2.61	2.7	2.7	K-Ohm	Different setting on NEC-TOKIN
VREF to GND	C8433	0.33	0.33	0.33	uF	
PWM3 to GND	R9097	56K	56K	56K	K-Ohm	Place 56K-Ohm to enable OSR
Rsequ	R9101, R9107, R9112	2.15	2.15	2.15	K-Ohm	R9112 = NO_ASM in 2-phase 37W
Rseries	R9099, R9106, R9113	2.94	2.94	2.94	K-Ohm	R9113 = NO_ASM in 2-phase 37W
Rpar	R9100, R9109, R9115	52.3	52.3	52.3	K-Ohm	R9115 = NO_ASM in 2-phase 37W
Csense	C985, C986, C987	150	150	150	nF	C987 = NO_ASM in 2-phase 37W
Rntc	RT17, RT18, RT19	10	10	10	K-Ohm	RT19 = NO_ASM in 2-phase 37W (NTC)
R9087	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
R9098	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
Q180	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
R9114	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
C8395	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
C8394	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
R9116	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
C8396	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
R9138	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
C8437	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
RT19	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
R9113	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
R9115	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
R9112	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
C987	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
L39	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
RJ117	NO_ASM	NO_ASM	NO_ASM	NO_ASM		
TC18	NO_ASM	NO_ASM	NO_ASM	NO_ASM		

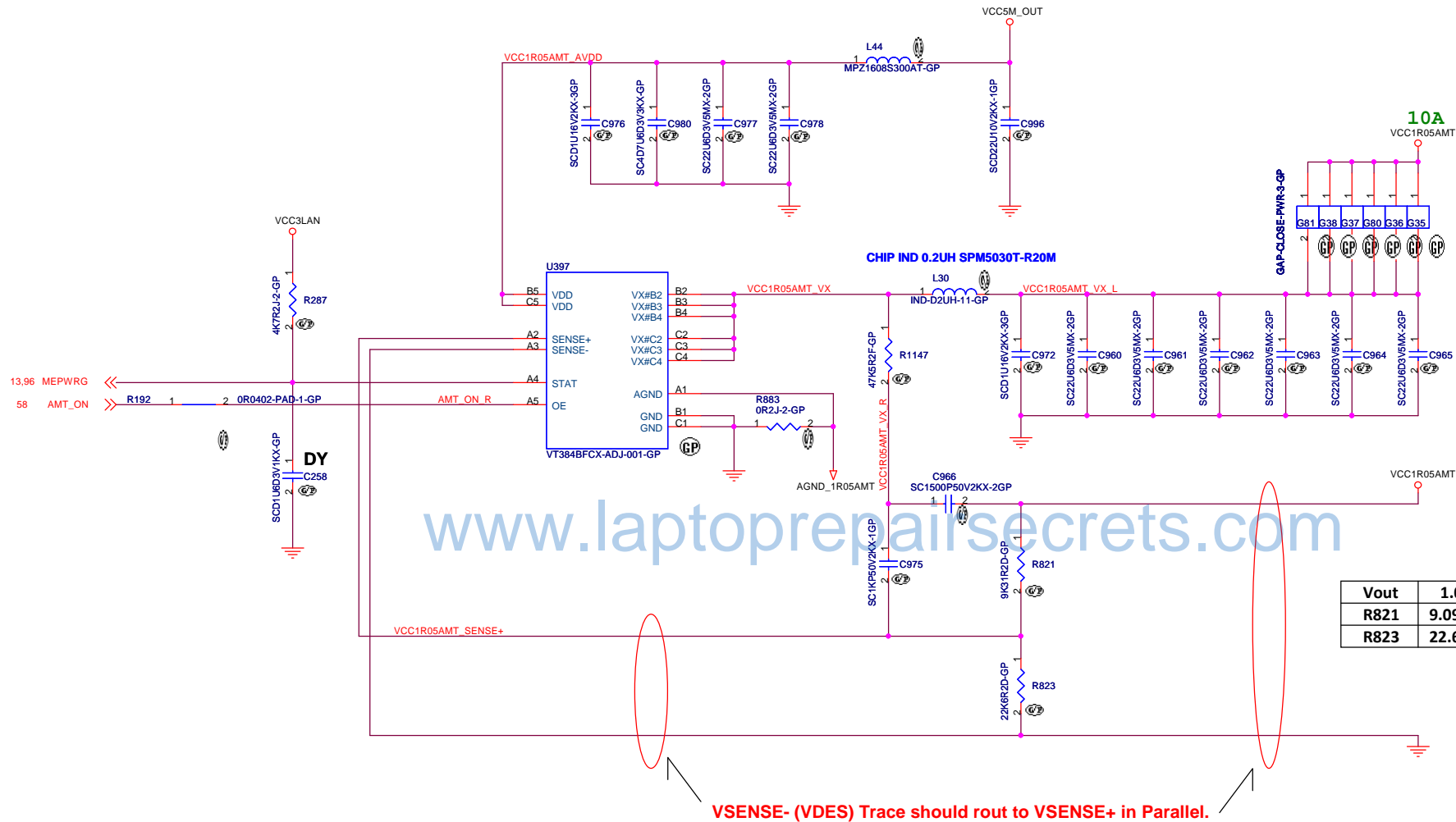
#### NOTES:

Min Over Current Limit is set to 70A for 37W and 110A for both 47W and 57W.  
Switching Frequency is set to 1MHz for 37W and 800KHz for 47W and 57W.  
Fine-tuning at motherboard evaluation level might still be needed to get the best performance.

Inductor MPCH0740LR15D (NEC-TOKIN) DCR=0.66mOhm

Connection	Component Name	37W 2 Phase	47W 3 Phase	57W 3 Phase	Unit	
IMON to OCF-I	R9079	180	97.6	86.6	K-Ohm	Different setting on TOKO
COMP to VREF	R9092	3	2.87	2.87	K-Ohm	Different setting on TOKO
DROOP to COMP	R9094 + C8386	10K + 330p	10K + 100p	10K + 100p		

<Variant Name>



Vout	1.052V	1.059V
R821	9.09K-ohm	9.31K-ohm
R823	22.6K-ohm	22.6K-ohm

↑  
LOGIC

<Variant Name>

緯創資通

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Title

**DC/DC VCC1R05AMT**

Size  
A3

Document Number

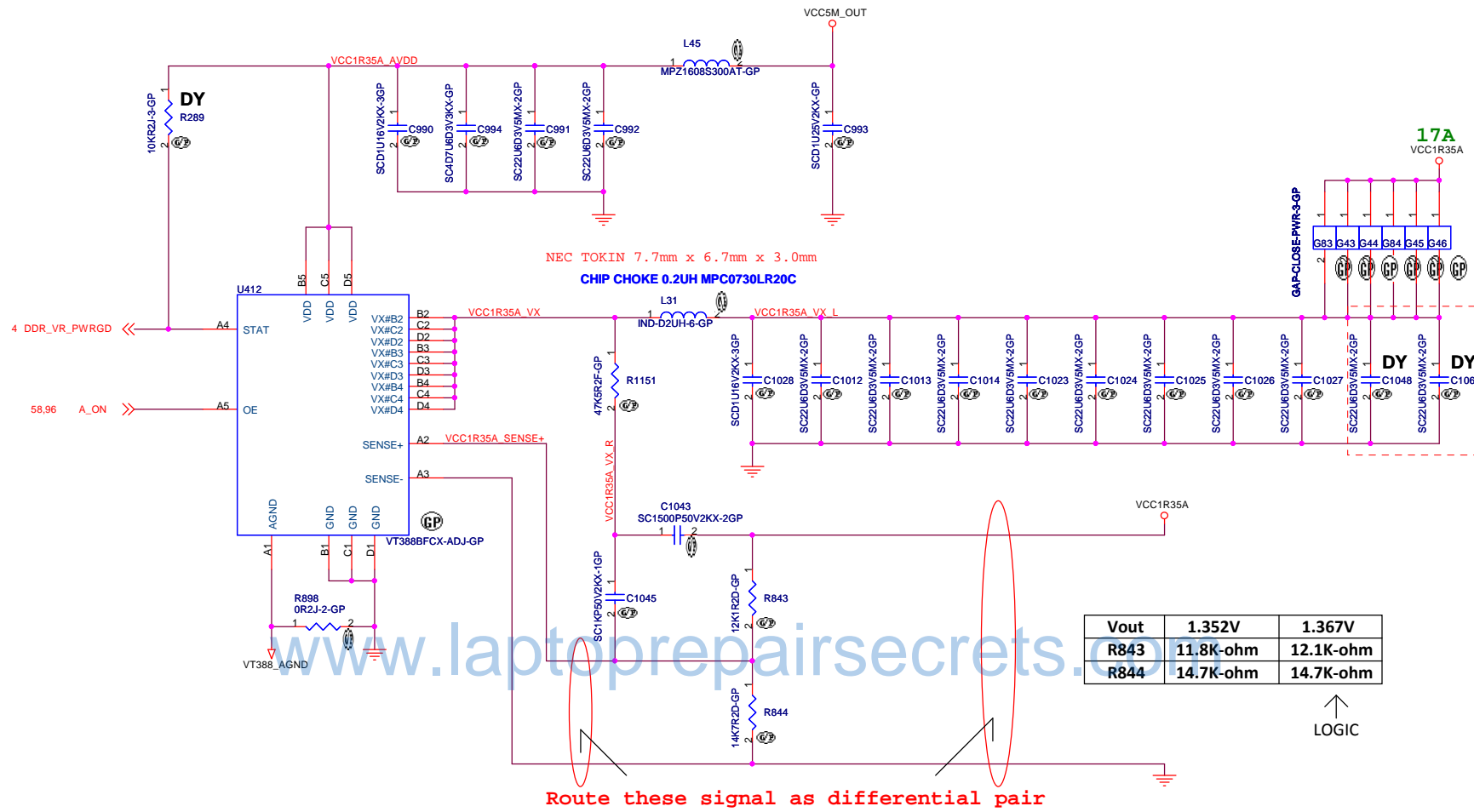
**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

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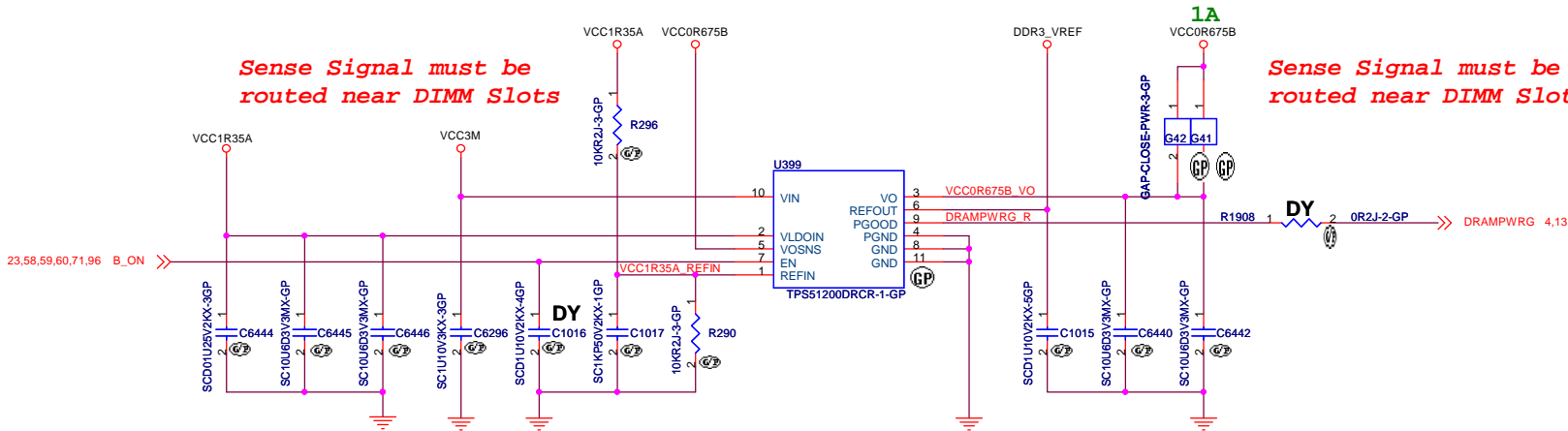


Vout	1.352V	1.367V
R843	11.8K-ohm	12.1K-ohm
R844	14.7K-ohm	14.7K-ohm

LOGIC

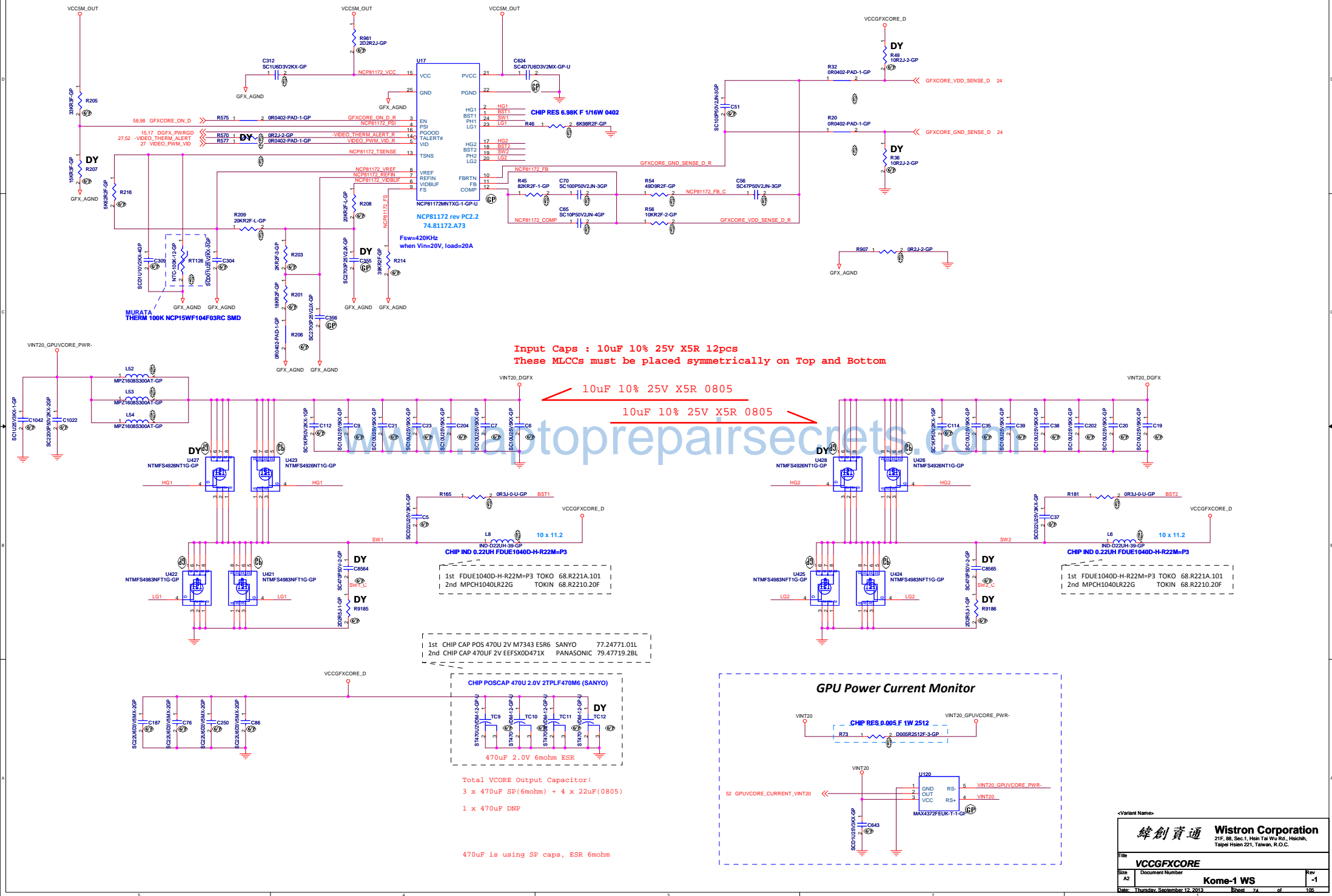
Sense Signal must be routed near DIMM Slots

Sense Signal must be routed near DIMM Slots

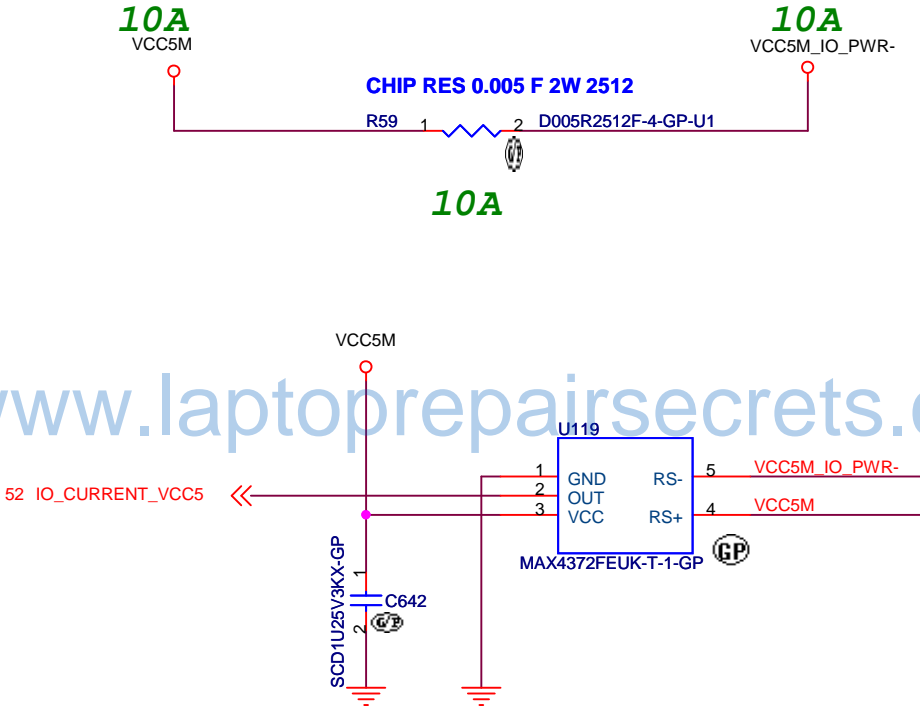








*This circuits to monitor on the current of VCC5 power rail  
relaed to System USB Ports, ODD, HDD and Thunderbolt.*



<Variant Name>

緯創資通

**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**CURRENT MONITOR I/O**

Size  
A4

Document Number

**Kome-1 WS**

Rev  
-1

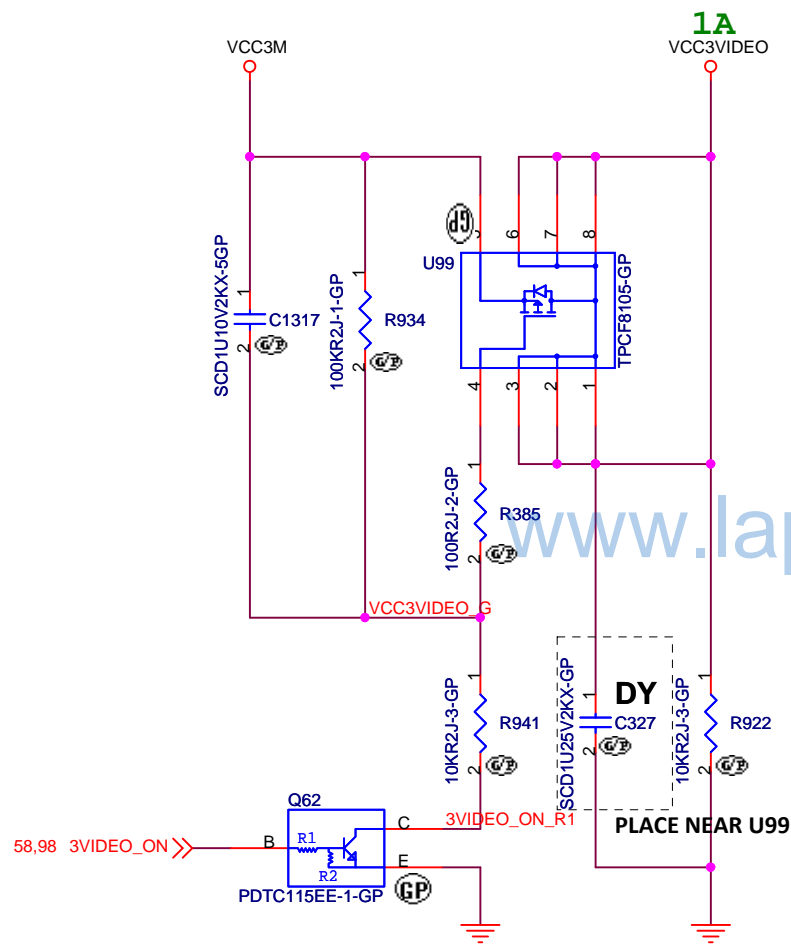
Date: Thursday, September 12, 2013

Sheet 75 of 105

- VCC3POC for Core and Integrated VR : 0.91A

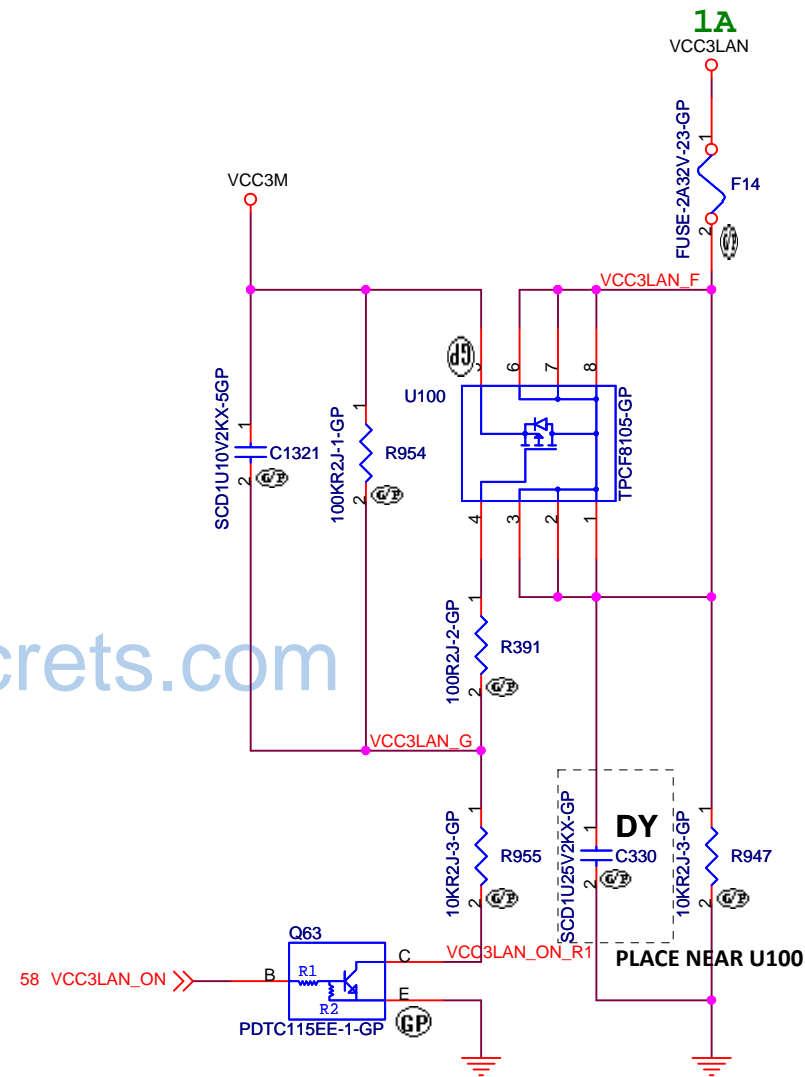


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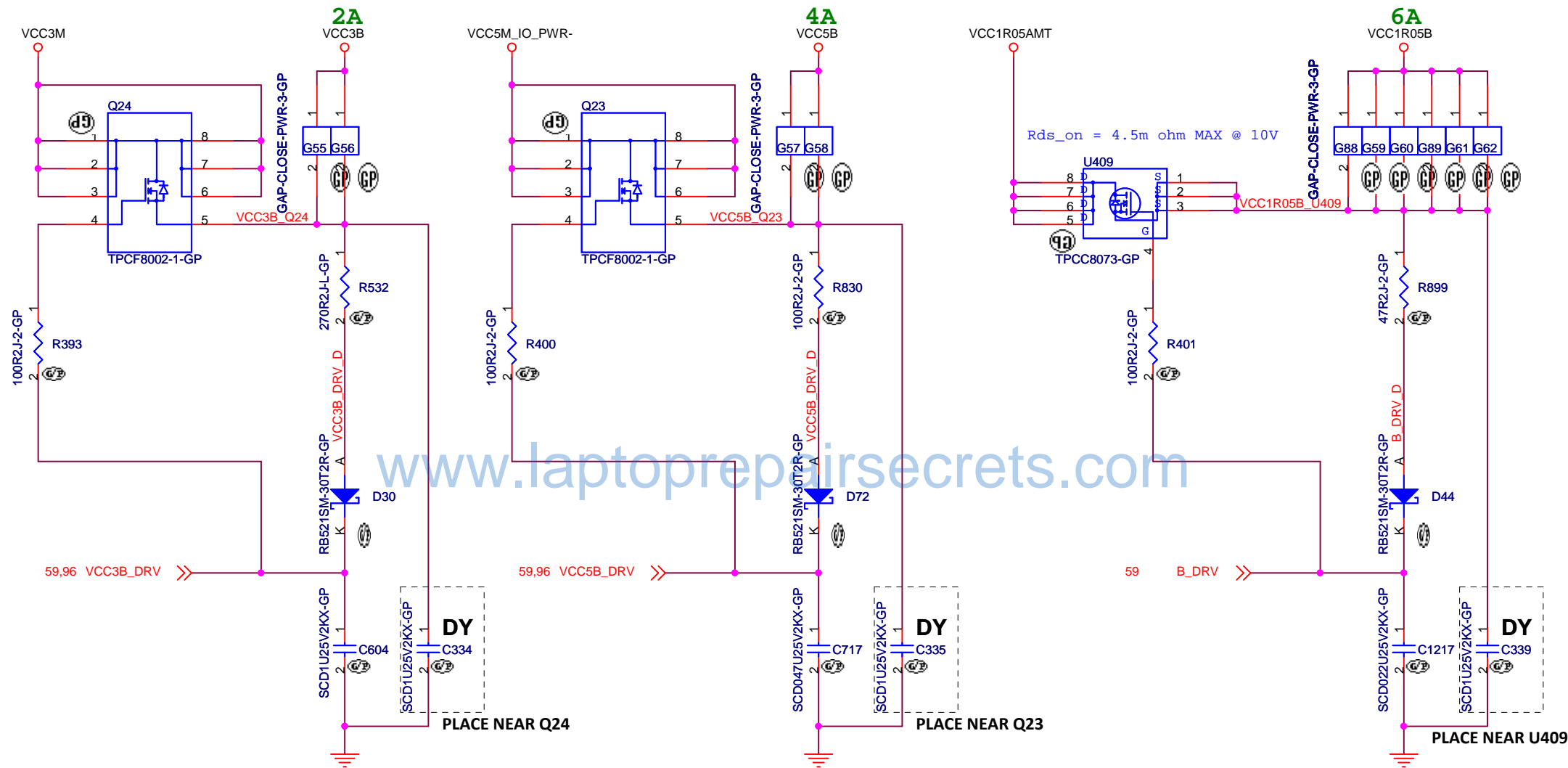
VCC3LAN provides  
to PCH, GBE and SPI deivce.

PCH requires 0.022A.  
GBE requires 0.5A max.  
SPI requires 0.04A(2pcs)



<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title	
LOAD SW VIDEO / LAN	
Size A4	<div>Document Number</div> <div>Kome-1 WS</div>
Date: Thursday, September 12, 2013	Sheet 77 of 105
Rev -1	



<Variant Name>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**LOAD SW VCCB**

Size  
A4

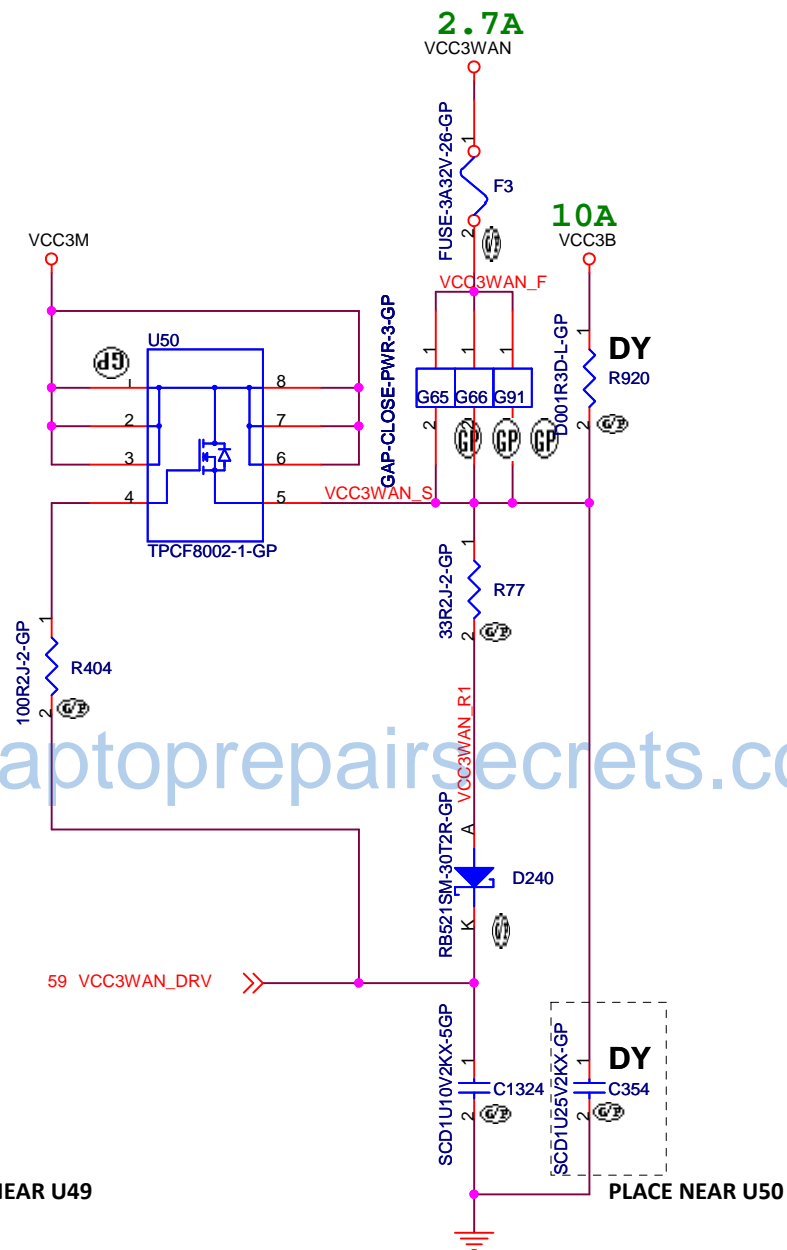
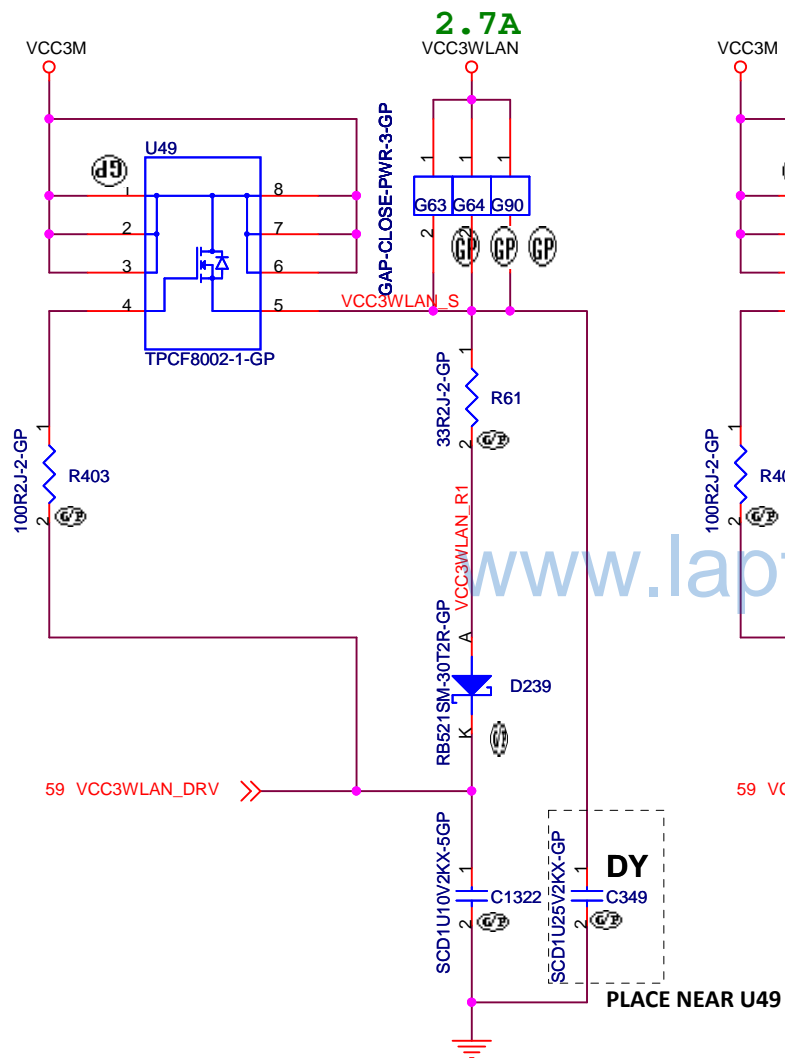
Document Number

**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

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<Variant Name>

緯創資通

**Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**LOAD SW WWAN WLAN ODD BAY**

Size  
A4

Document Number

**Kome-1 WS**

Rev  
-1

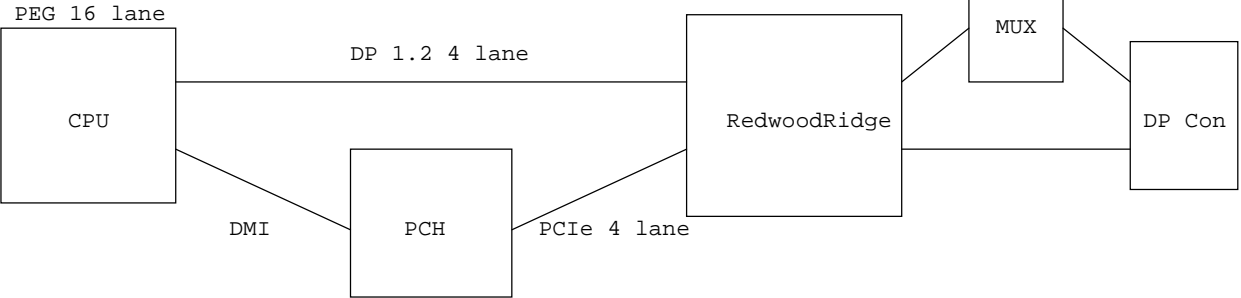
Date: Thursday, September 12, 2013

Sheet 79 of 105

Redwood Ridge device has three kind of SKU.

Code Name	Product Number	Display Port Configuration	PCIe	Package	TDP
Redwood Ridge 4C	DSL4510	1.1a, 2x sink, 1x source	x4 Gen2	12x12mm	3.1W
Redwood Ridge 2C (12x12)	DSL4410	1.1a, 2x sink, 0x source	x4 Gen2	12x12mm	2.3W
Redwood Ridge 2C (10x10)	DSL4310	1.1a, 2x sink, 0x source	x4 Gen2	10x10mm	2.3W

This Project will use redwood Ridge 2C, because TDP target value will be reduced to 2W.

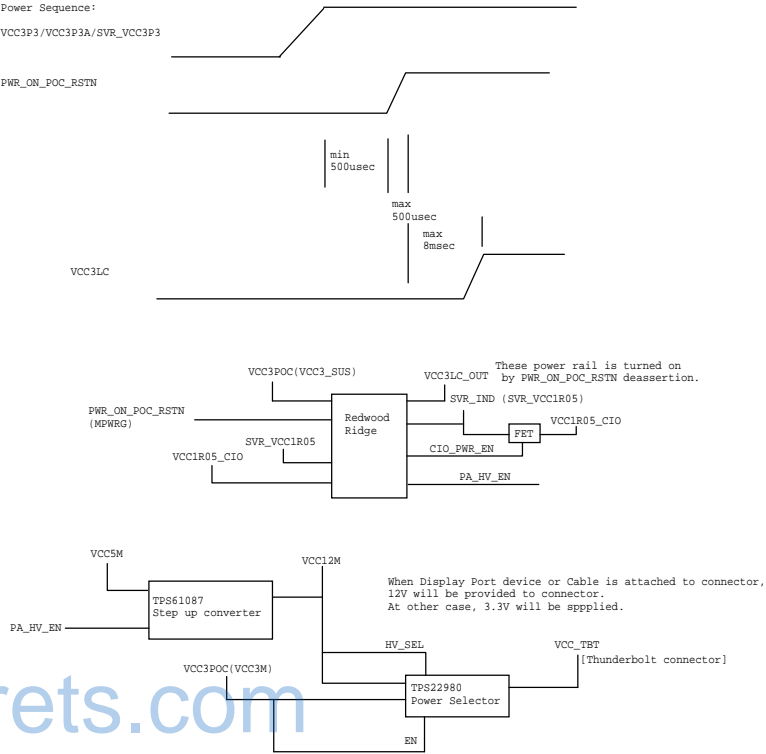


Display Port/Thunderbolt Connector

Legacy Display Port [mini DP]		Thunderbolt Port		Implementation	
Pin	Description	Pin	Description	Pin	
1	GND	1	PWR IN	1	Add Cap
2	HPD	2	HPD	2	HPD with Buffer?
3	LANE 0P	3	HD2CA OP [OUT]	3	CIO Port 0 Bus Switch in Redwood Ridge for ML0P/HD2CA0P
4	CONFIG 1	4	CA2HD OP [IN]	4	CIO Port 0 in Redwood Ridge for CA2HA0P and buffer for Config 1
5	LANE 0N	5	HD2CA ON [OUT]	5	CIO Port 0 Bus Switch in Redwood Ridge for ML0N/HD2CA0N
6	CONFIG 2	6	CA2HD ON [IN]	6	CIO Port 0 in Redwood Ridge for CA2HD0N and buffer for Config 2
7	GND	7	GND	7	GND
8	GND	8	GND	8	GND
9	LANE 1P	9	LSTX (Low Speed Control Output)	9	External Bus Switch for ML1P/LSTX
10	LANE 3P	10	RSV (Pulldown with 50ohm)	10	DP port in Redwood Ridge for ML3P
11	LANE 1N	11	LSRX (Low Speed Control Input)	11	External Bus Switch for ML1N/LSRX
12	LANE 3N	12	RSV (Pulldown with 50ohm)	12	DP port in Redwood Ridge for ML3N
13	GND	13	GND	13	GND
14	GND	14	GND	14	GND
15	LANE 2P	15	HD2CA 1P	15	CIO Port 1 Bus Switch in Redwood Ridge for ML2P/HD2CA1P
16	AUXP	16	CA2HD 1P	16	CIO Port 1 in Redwood Ridge for CA2HD1P
17	LANE 2N	17	HD2CA 1N	17	CIO Port 1 Bus Switch in Redwood Ridge for ML2N/HD2CA1N
18	AUXN	18	CA2HD 1N	18	CIO Port 1 in Redwood Ridge for CA2HD1N
19	PWR RET	19	PWR RTN	19	GND
20	PWR	20	PWR OUT [Supply to device]	20	Power from DCDC

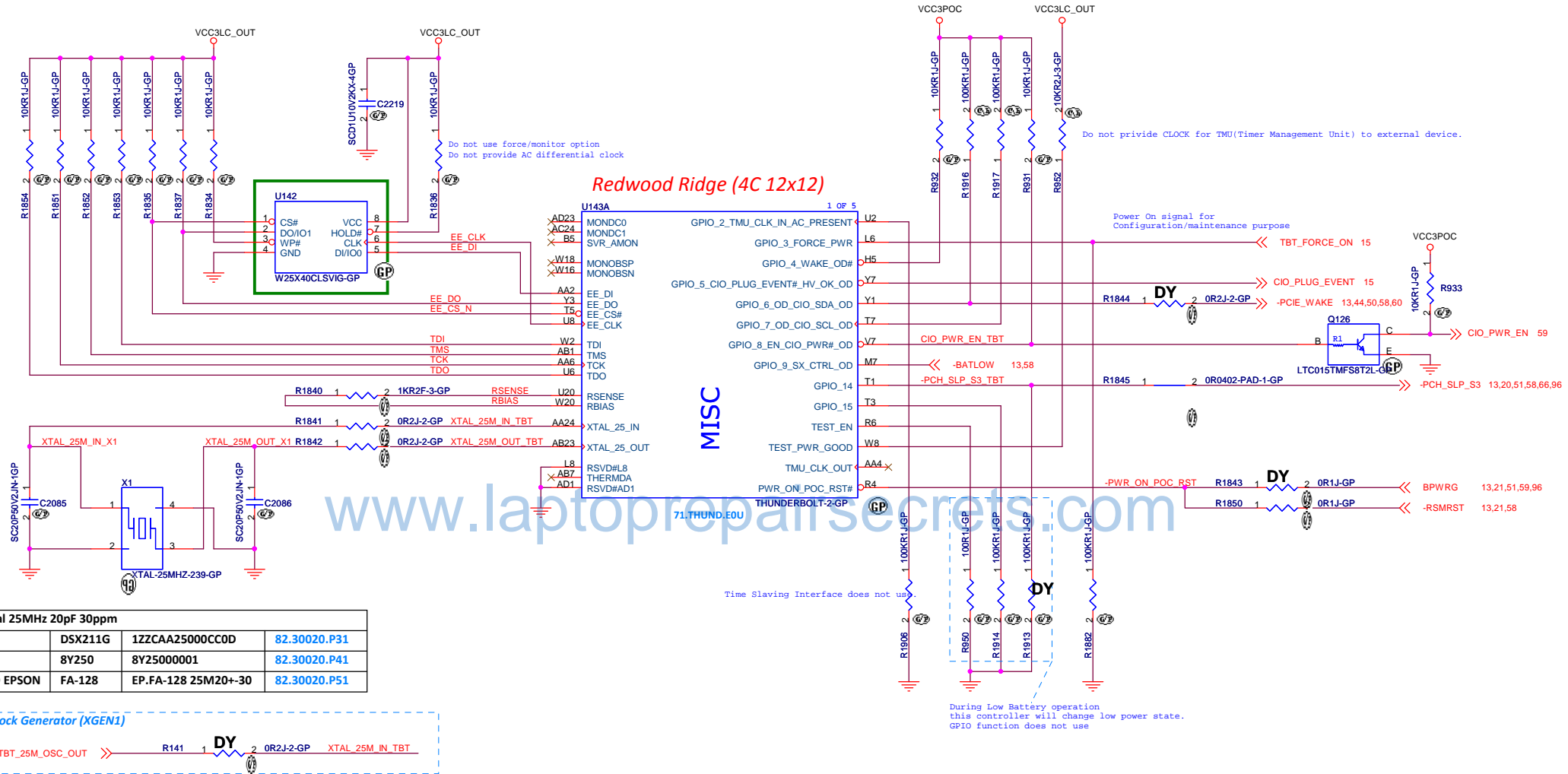
The way to distinguish Legacy Display Port or Thunderbolt  
- Thunderbolt controller must switch the function based on pulldown on HPD/Config1/Config2/LSTX/LSRX.

PCIe 1x4 Configuration is used for Redwood Ridge as outer mode.



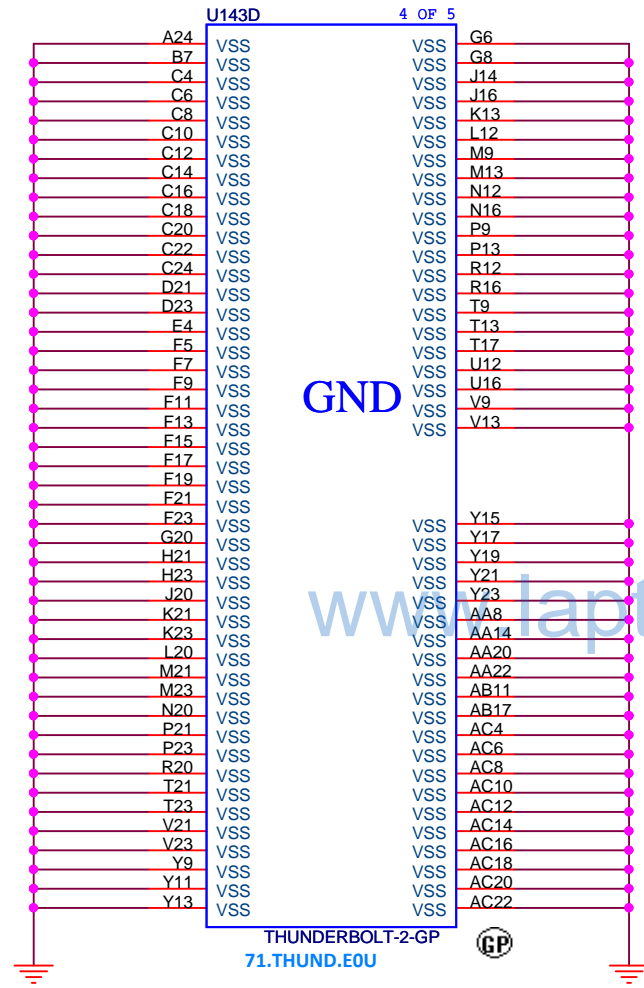


Thunderbolt EEPROM (only WS): U142		
Winbond	W25X40CLSVIG	72.25X40.009





# Redwood Ridge (4C 12x12)



<Variant Name>

緯創資通

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Title

**Thunderbolt Redwood GND (4/6)**

Size  
A4

Document Number

**Kome-1 WS**

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-1

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# Redwood Ridge (4C 12x12)



<Variant Name>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Thunderbolt Redwood PCIE-CPU (5/6)**

Size  
A4

Document Number

**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

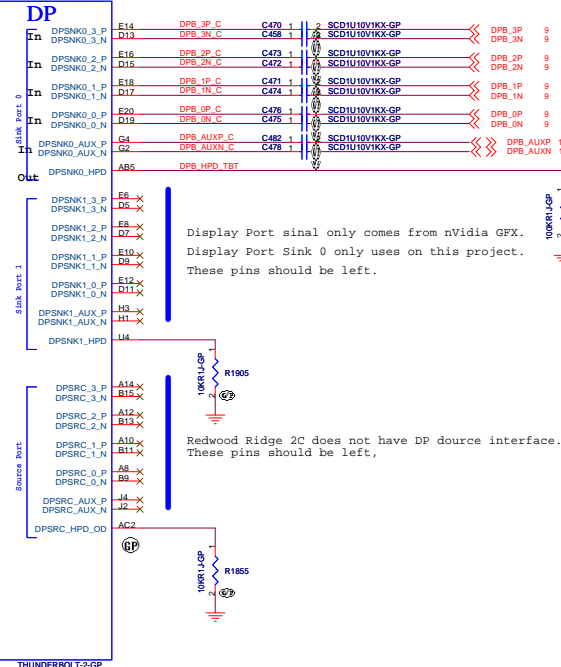
Sheet 84 of 105

C10		DP	
PA.DPSRC_3,P PA.DPSRC_3,N	Out	In	DP.SNK0_3,P DP.SNK0_3,N
PA.DPSRC_1,P	Out	In	DP.SNK0_2,P
PA.AUX,P PA.AUX,N	In/Out	In	DP.SNK0_1,P DP.SNK0_1,N
PA.DPSRC_HPD		In	DP.SNK0_0,P DP.SNK0_0,N
PA.CIO2_TX,P.DPSRC_0,P PA.CIO2_TX,N.DPSRC_0,N	Out	In	DP.SNK0_AUX,P DP.SNK0_AUX,N
PA.CIO0_RX,P PA.CIO0_RX,N	In	Out	DP.SNK0_HPD
PA.CONFIG1_CIO_0,LSOE PA.CONFIG2_CIO_0,LSOE	In/Out		DP.SNK1_3,P DP.SNK1_3,N
PA.CIO1_TX,P.DPSRC_2,P PA.CIO1_TX,N.DPSRC_2,N	Out		DP.SNK1_2,P DP.SNK1_2,N
PA.CIO1_RX,P PA.CIO1_RX,N	In		DP.SNK1_1,P DP.SNK1_1,N
PA.LSTX_CIO_1,LSOE PA.LSRX_CIO_1,LSOE	In/Out		DP.SNK1_0,P DP.SNK1_0,N
GPIO_0_PA_HY_EN_BYP0 GPIO_10_PA_CIO_SEL_BYP1 GPIO_12_PA_PB_PWDRN_BYP2	Out Out Out		DP.SNK1_AUX,P DP.SNK1_AUX,N
PB.DPSRC_3,P PB.DPSRC_3,N			DP.SNK1_HPD
PB.DPSRC_1,P PB.DPSRC_1,N			
PB.AUX,P PB.AUX,N			
PB.DPSRC_HPD			
PB.CIO2_TX,P.DPSRC_2,P PB.CIO2_TX,N.DPSRC_2,N			DP.SRC_3,P DP.SRC_3,N
PB.CIO2_RX,P PB.CIO2_RX,N			DP.SRC_2,P DP.SRC_2,N
PB.CONFIG1_CIO_2,LSOE PB.CONFIG2_CIO_2,LSOE	In/Out		DP.SRC_1,P DP.SRC_1,N
PB.CIO3_TX,P.DPSRC_2,P PB.CIO3_TX,N.DPSRC_2,N			DP.SRC_0,P DP.SRC_0,N
PB.CIO3_RX,P PB.CIO3_RX,N			DP.SRC_AUX,P DP.SRC_AUX,N
PB.LSTX_CIO_3,LSOE PB.LSRX_CIO_3,LSOE	In/Out		DP.SRC_HPD_OD
GPIO_1_PB_HY_EN_BYP0 GPIO_11_PB_CIO_SEL_BYP1 GPIO_13_PB_PD_PWDRN_BYP2	Out Out Out		

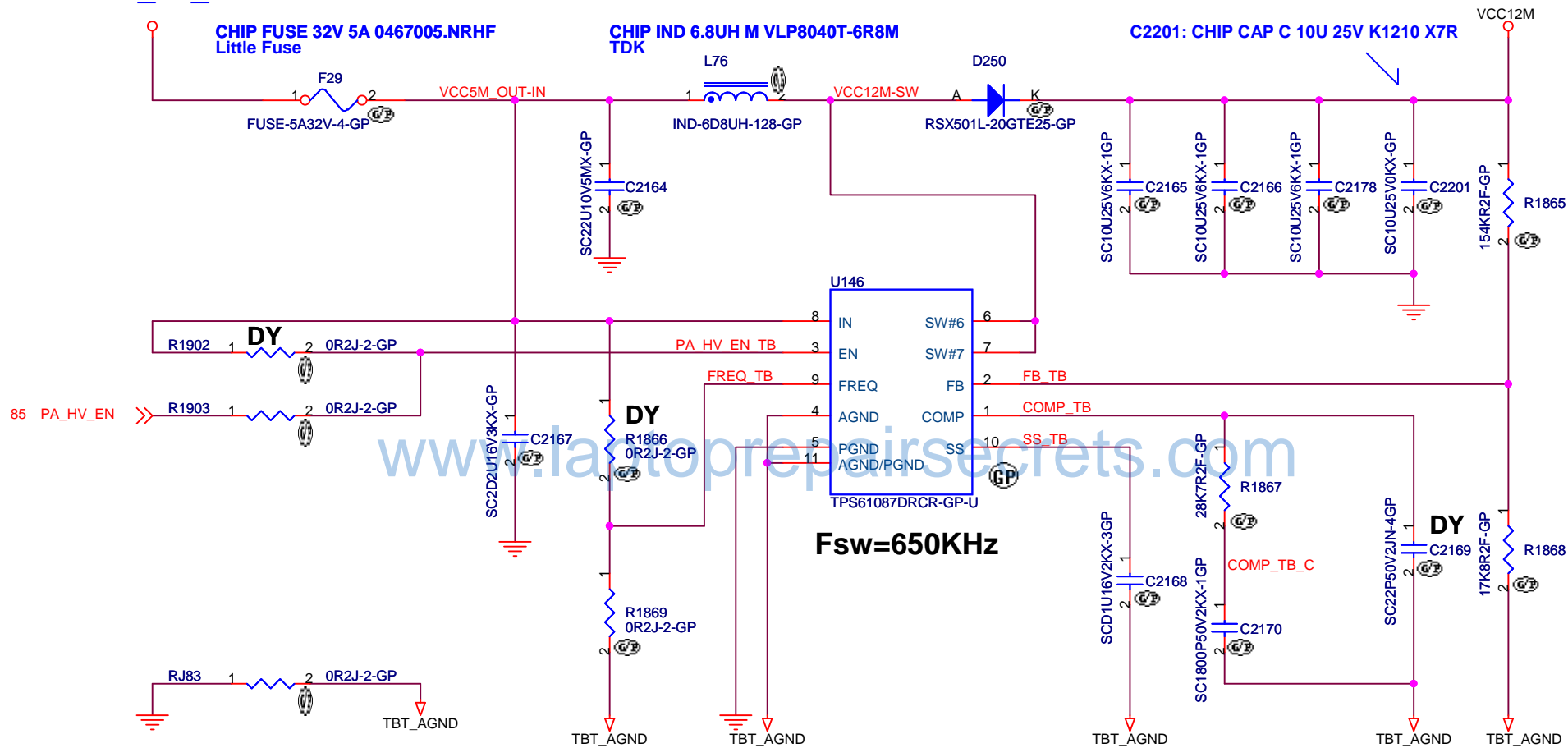
71.THUND.EU
THUNDERBOLT-2-GP

Display Port sinal only comes from nVidia GFX.  
Display Port Sink 0 only uses on this project.  
These pins should be left.

Redwood Ridge 2C does not have DP dource interface.  
These pins should be left,



# VCC5M\_IO\_PWR-



<Variant Name>

緯創資通

**Wistron Corporation**

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Title

**Thunderbolt VCC12M**

Size  
A4

Document Number

**Kome-1 WS**

Rev  
-1

Date: Thursday, September 12, 2013

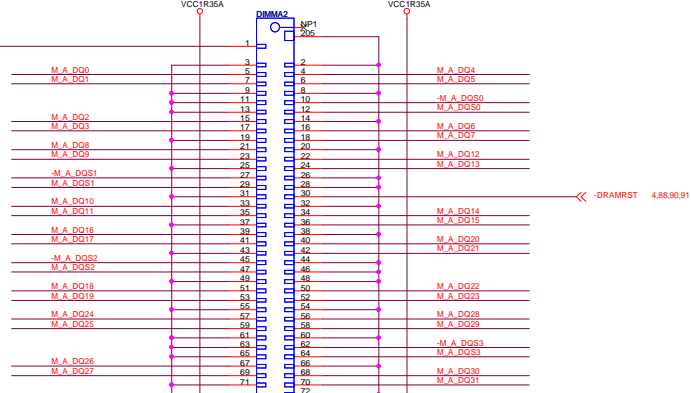
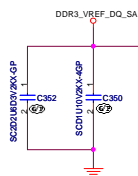
Sheet 86 of 105

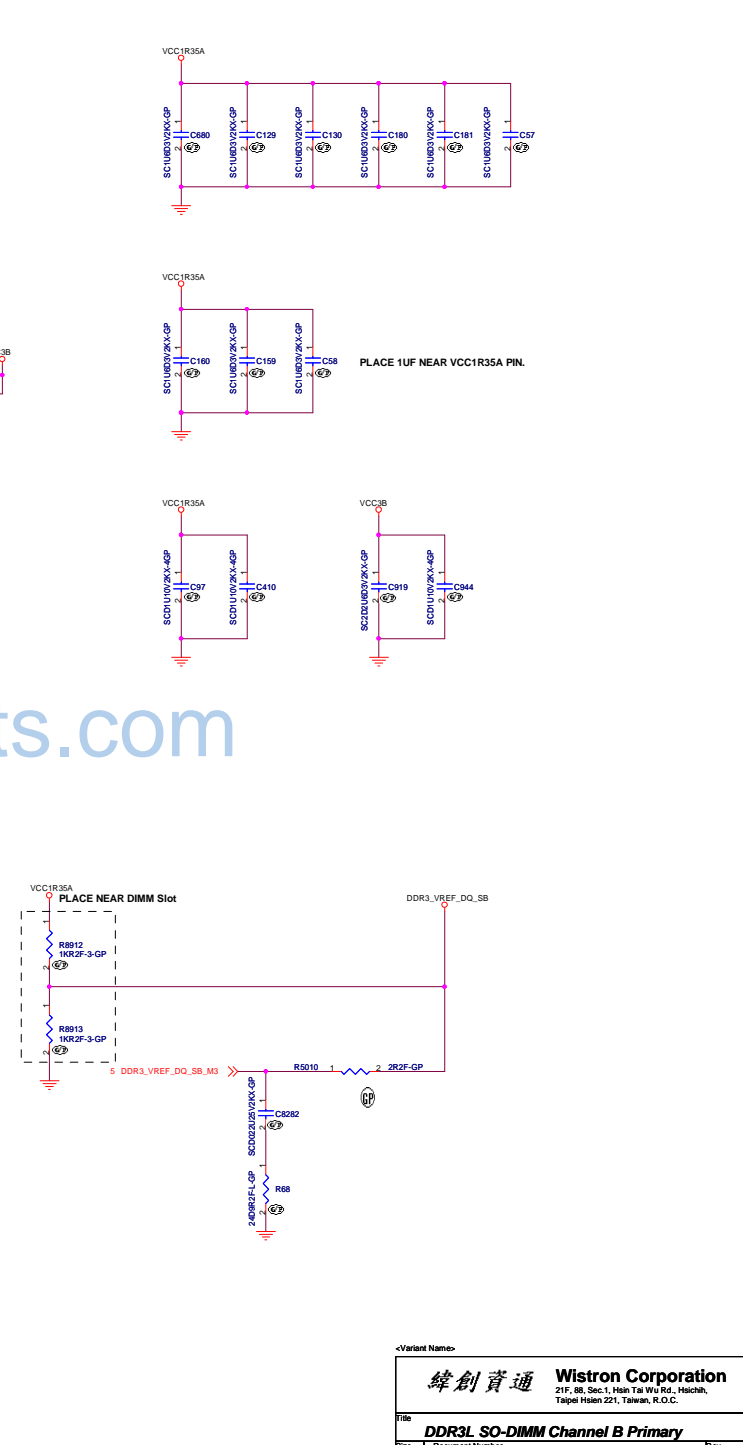
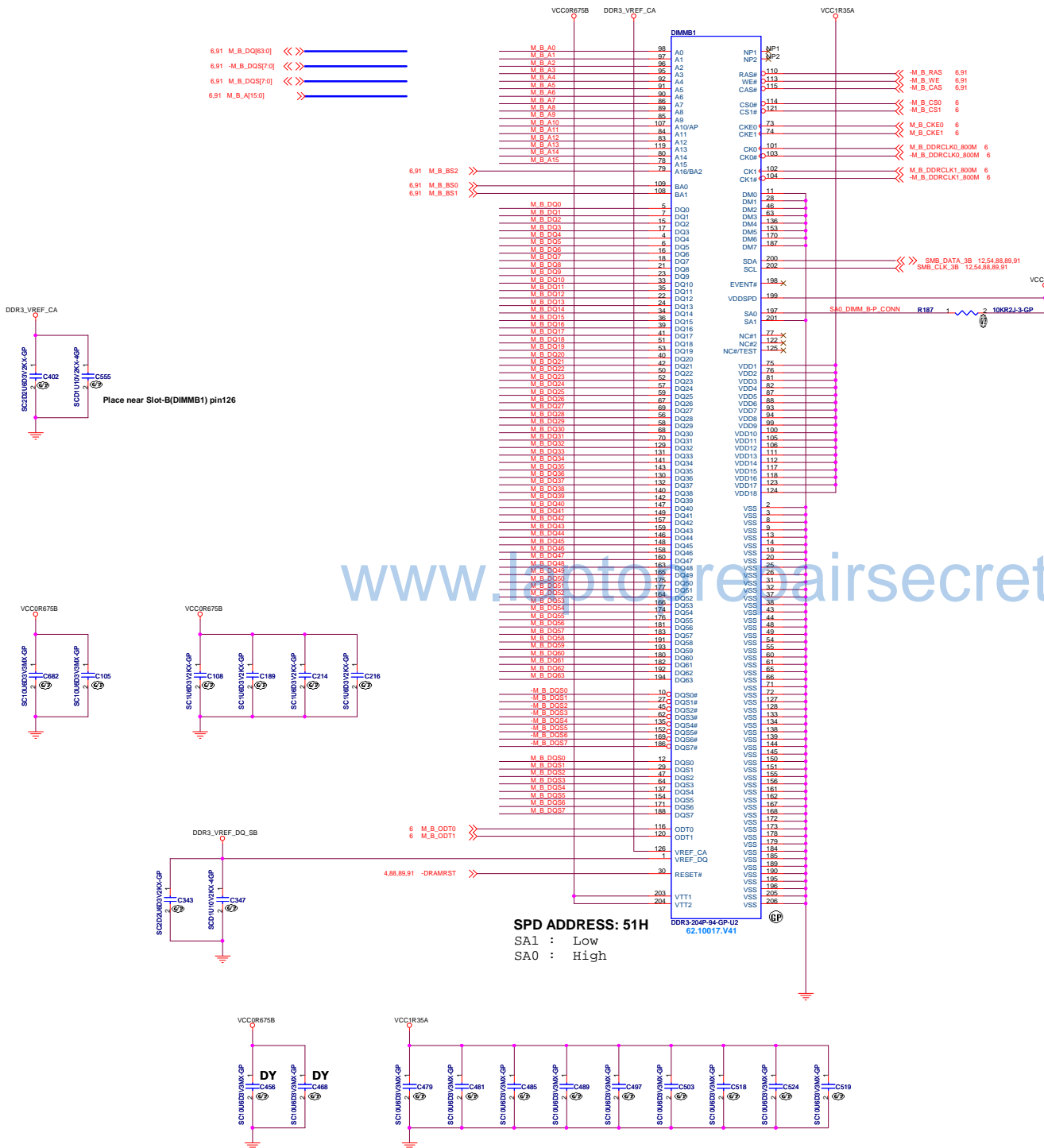






5.88 M\_A\_DQ[63:0] <<>  
 5.88 -M\_A\_DQS[7:0] <<>  
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 5.88 M\_A\_A[15:0] <<>







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<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
DIMM Topology		
Size	Document Number	Rev
A4	Kome-1 WS	-1
Date:	Wednesday, July 17, 2013	Sheet 92 of 105

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<Variant Name>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

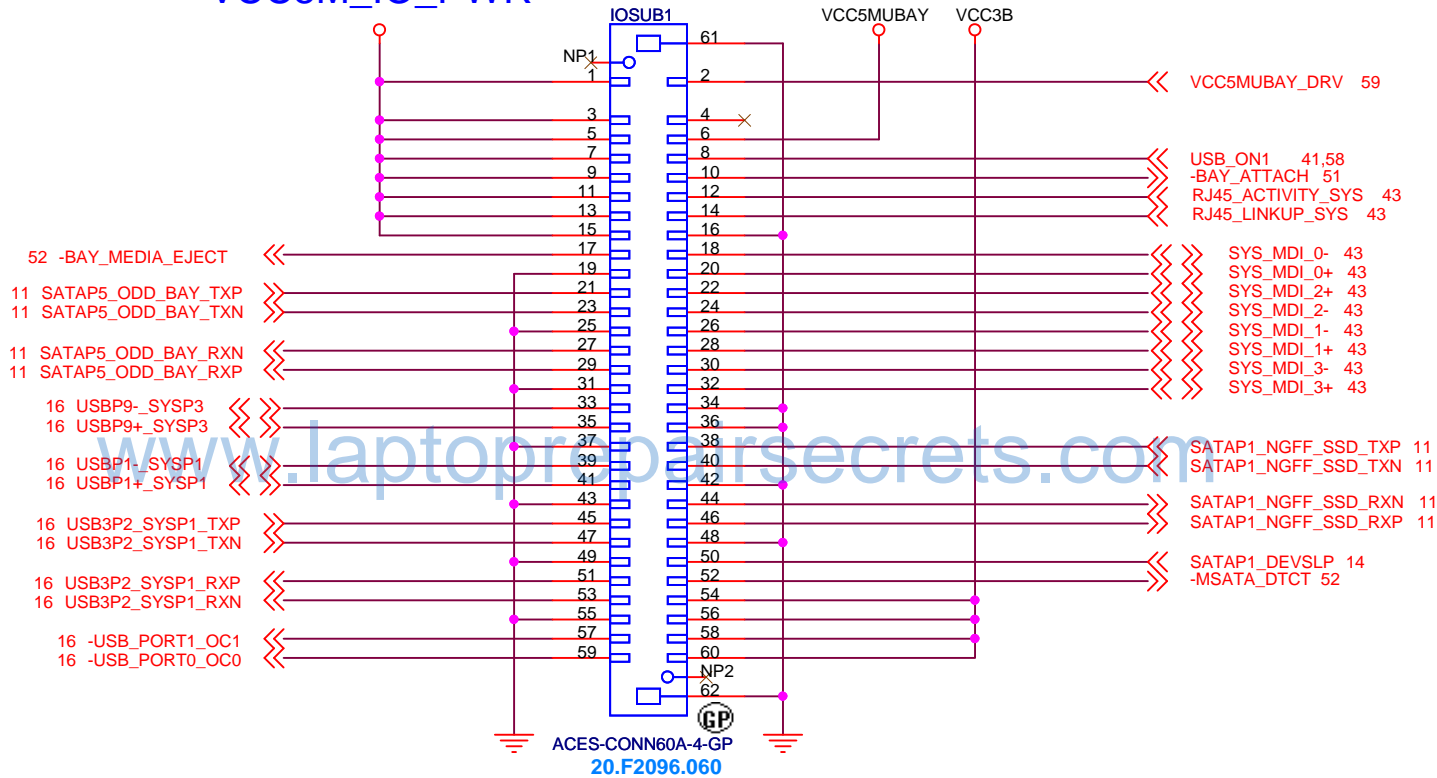
Title		
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Size	Document Number	Rev
A4	Kome-1 WS	-1
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Near IO SubCard CONN: IOSUB1 (p.094)



I/O SubCard Interface Connector

VCC5M\_IO\_PWR-



60-pins Board to Board Connector

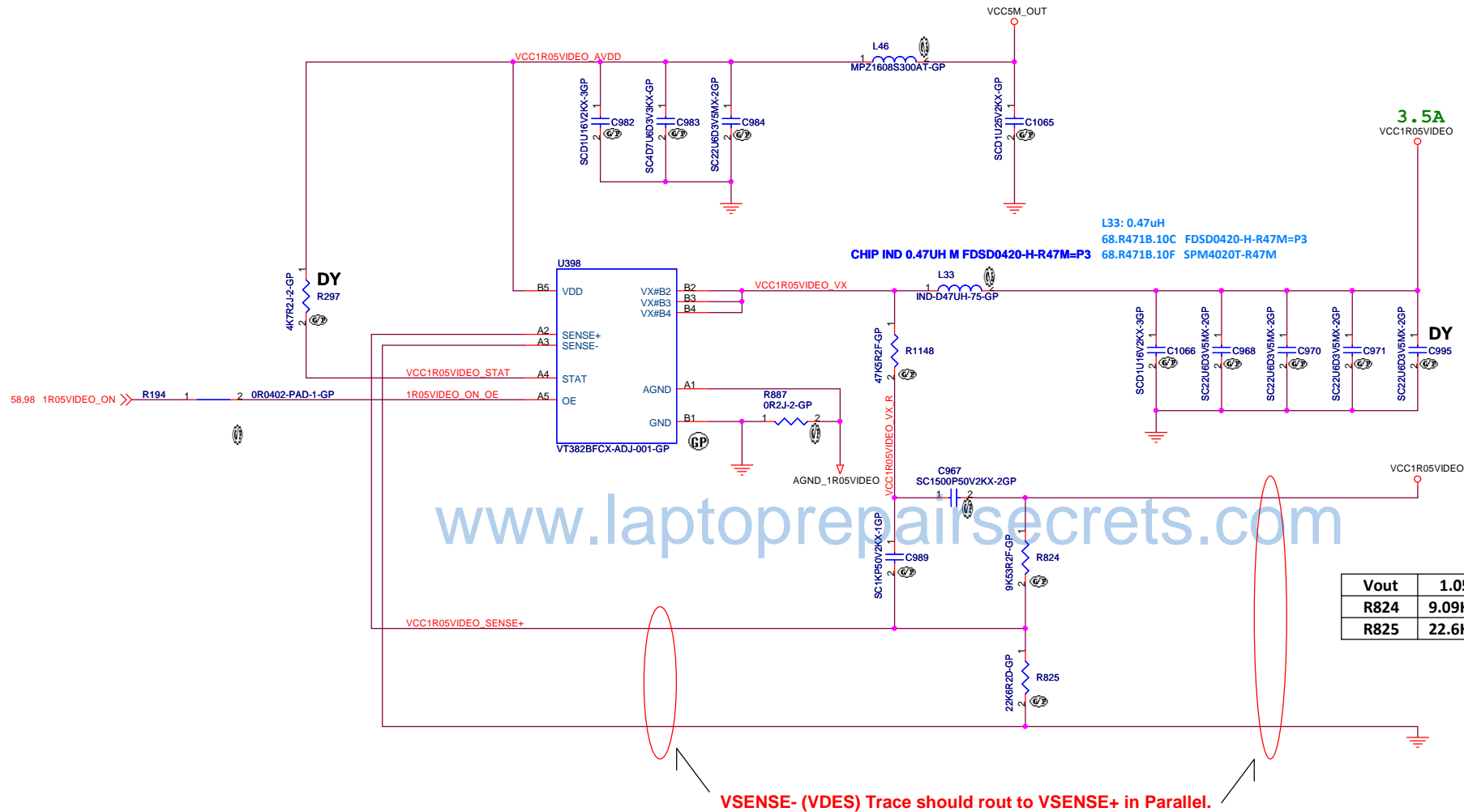
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緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
I/O SubCard Interface

Size A4 Document Number Kome-1 WS Rev -1

Date: Thursday, September 12, 2013 Sheet 94 of 105



Vout	1.052V	1.059V	1.066V
R824	9.09K-ohm	9.31K-ohm	9.53K-ohm
R825	22.6K-ohm	22.6K-ohm	22.6K-ohm

↑  
LOGIC

<Variant Name>

**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

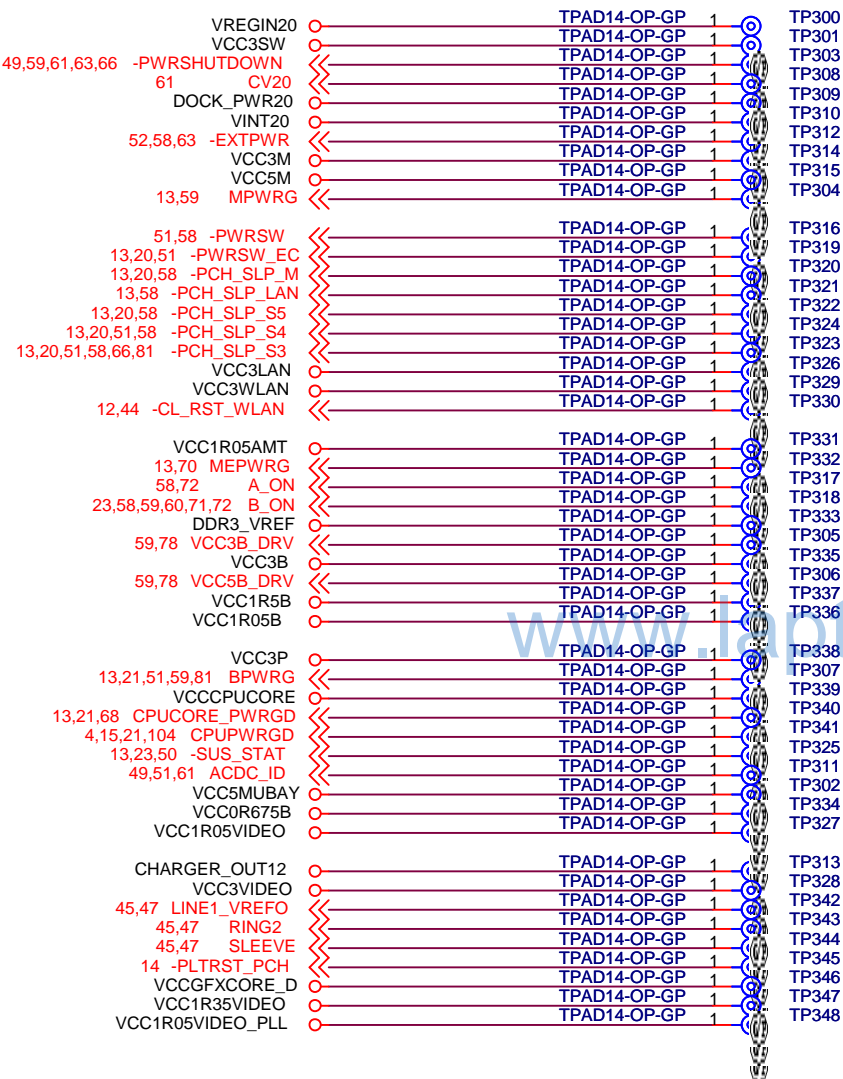
Title **DC/DC VCC1R05VIDEO**

Size A3 Document Number **Kome-1 WS** Rev **-1**

Date: Thursday, September 12, 2013 Sheet 95 of 105

TOP VIEW Test Pad 14Mils

ZZ.PAD14.001



<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <b>Test Pad</b>		
Size A4	Document Number <b>Kome-1 WS</b>	Rev <b>-1</b>
Date: Thursday, September 12, 2013		Sheet 96 of 105

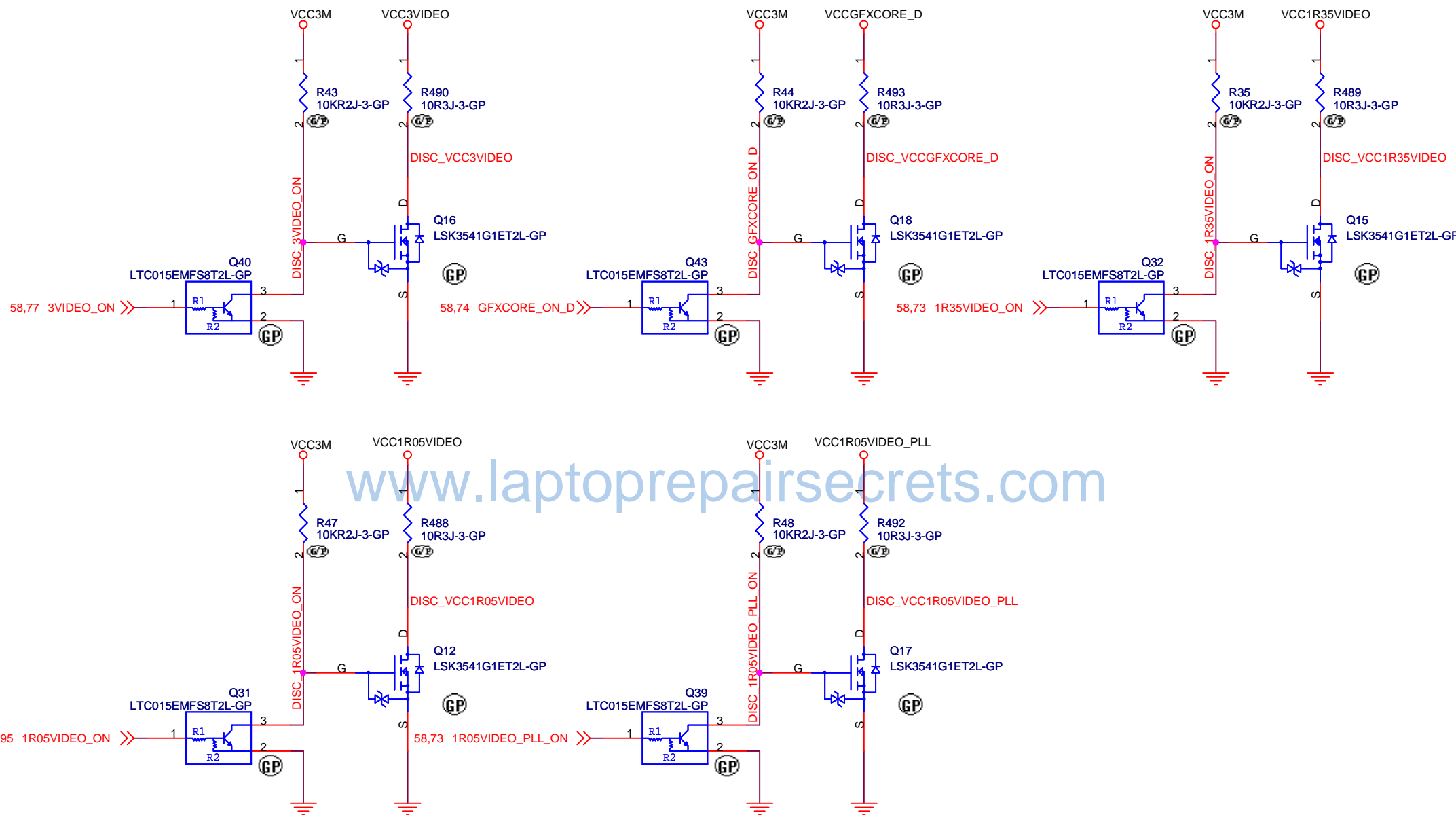


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<Variant Name>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
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Size	Document Number	Rev
A4	Kome-1 WS	-1
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<Variant Name>

緯創資通

**Wistron Corporation**

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Title

**Discharge Circuit**

Size  
A4

Document Number

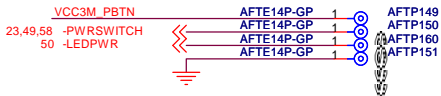
**Kome-1 WS**

Rev  
-1

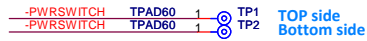
Date: Thursday, September 12, 2013

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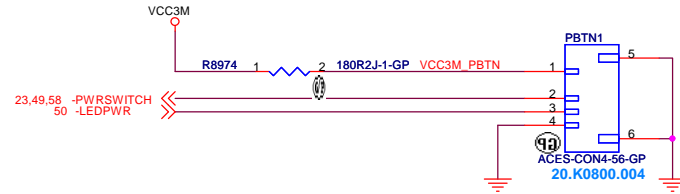
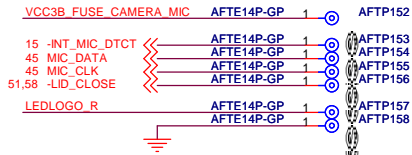
### Near Power SW CONN: PBTN1 (p.099)



### Near Power SW CONN: PBTN1 (p.099)



### Near Camera CONN: CMR1 (p.099)

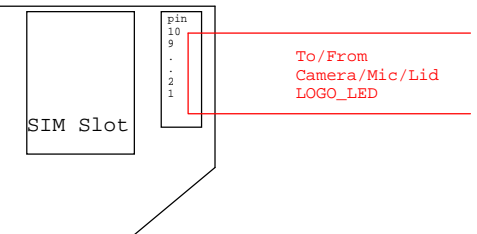
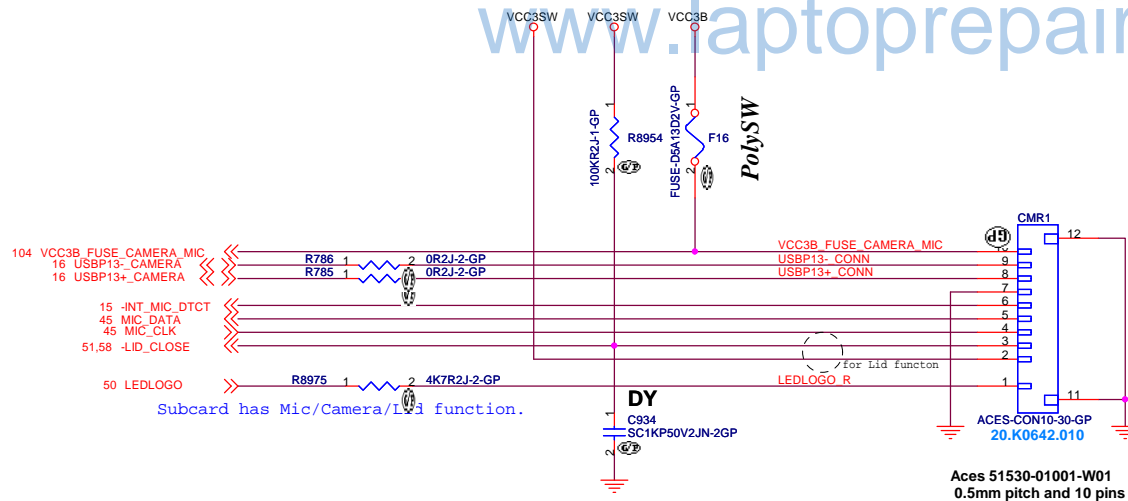


Normal type SMT connector  
Terminal is placed on PCB side

OR

Reversed Type connector  
Terminal is placed on opposit side from PCB

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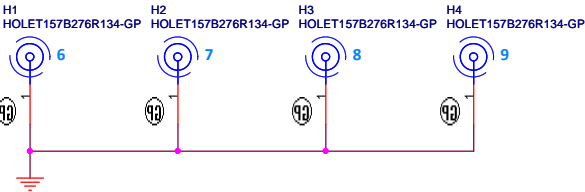
<Variant Name>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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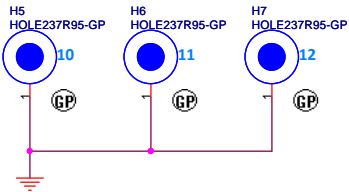
Title			
SubCard Power SW, Camera/Mic/Lid Interface			
Size	Document Number	Rev	
A3	Kome-1 WS	-1	
Date: Thursday, September 12, 2013		Sheet 99	of 105

TOP VIEW

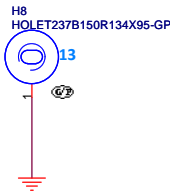
ZZ.SCREW.091



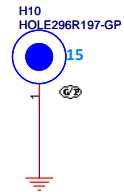
ZZ.00PAD.921



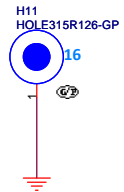
ZZ.SCREW.B31



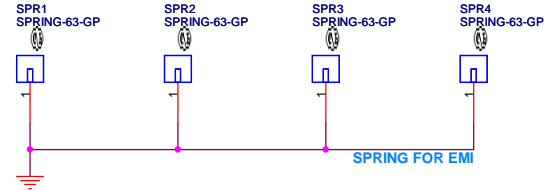
ZZ.00PAD.3Q1



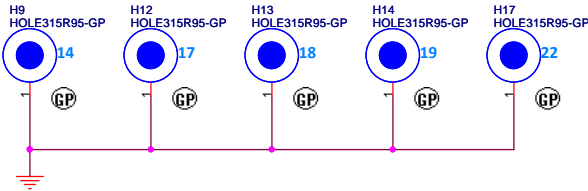
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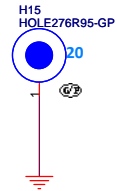
34.4Y806.001



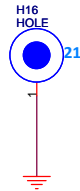
ZZ.00PAD.911



ZZ.SCREW.701



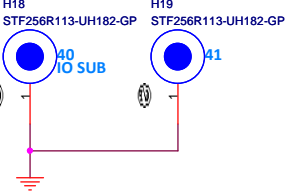
ZZ.0HOLE.XXX



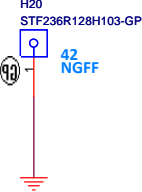
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BOTTOM VIEW

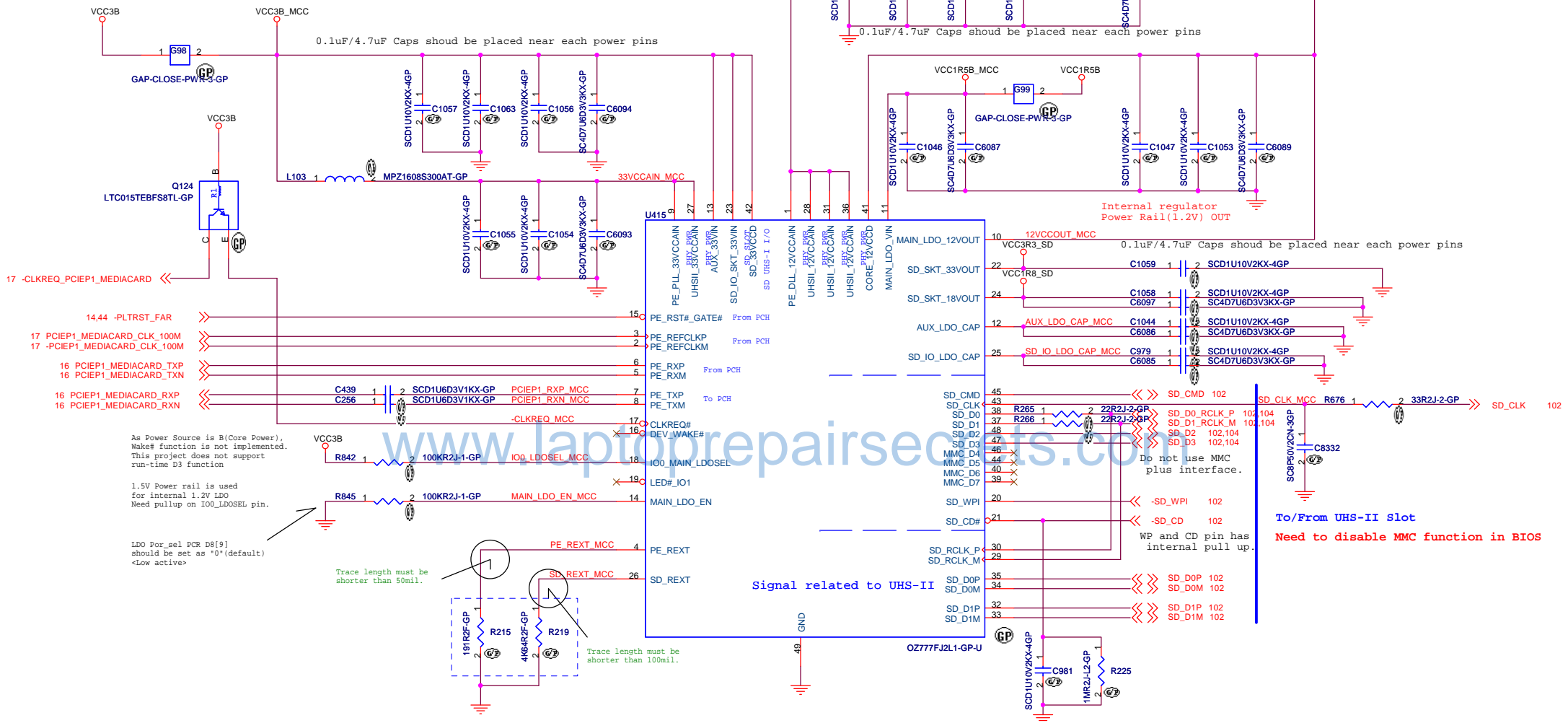
34.4JN01.001



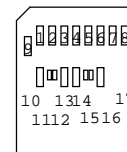
34.4Z003.201



The distance between Analog Power pin and Power filter must be set within 200mil



Bottom View



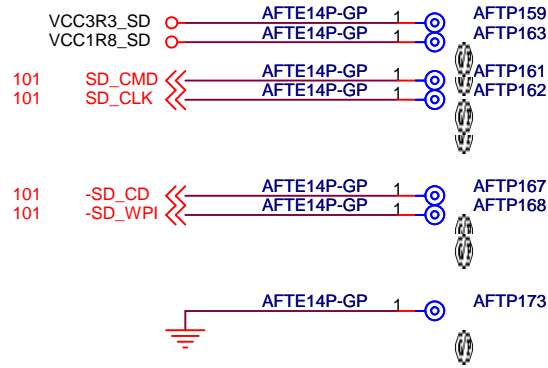
UHS II Interface  
4 VDD1 3.3V  
7 RCLKP  
8 RCLKM  
10 VSS3  
11 D0P  
12 D0M  
13 VSS4  
14 VDD2 1.8V  
15 D1M  
16 D1P  
17 VSS5

UHS I Interface  
1 CD/DAT3  
2 CMD  
3 VSS1  
4 VDD 3.3V  
5 CLK  
6 VSS2  
7 DAT0  
8 DAT1  
9 DAT2

<Variant Name>

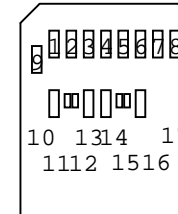
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Media Card Controller</b>		
Size A3	Document Number <b>Kome-1 WS</b>	Rev <b>-1</b>
Date: Thursday, September 12, 2013 Sheet 101 of 105		

## Near MediaCard Slot: MCS1 (p.102)

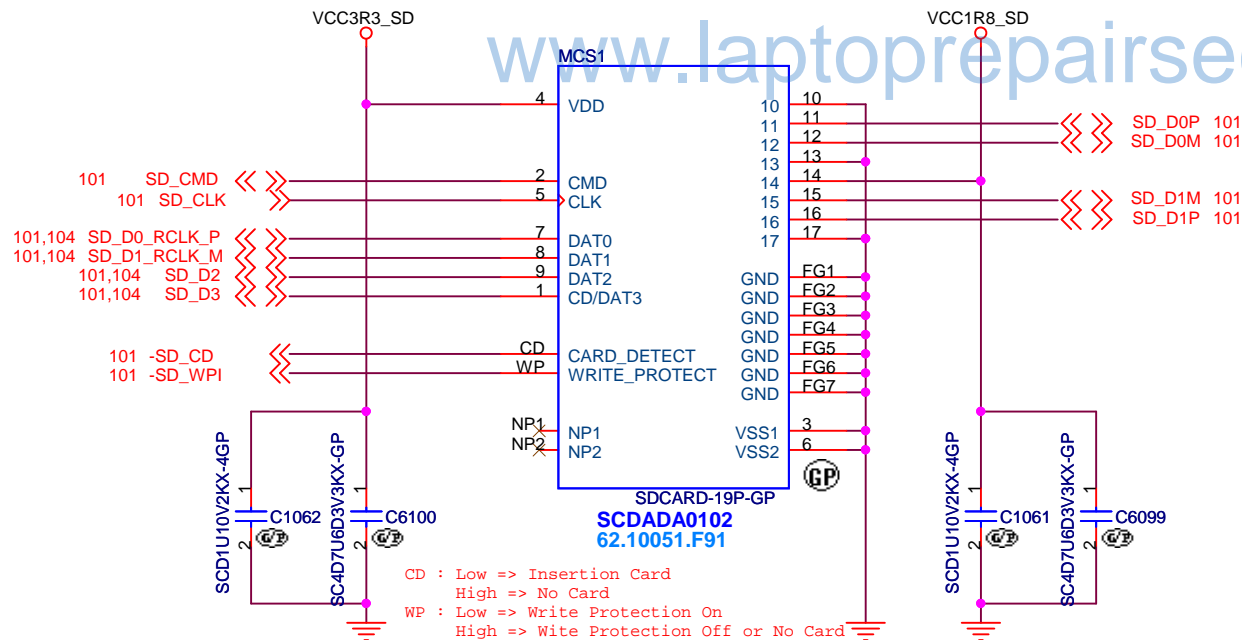


Pin No	SD Mode	UHS II Mode
1	CD/DAT3	
2	CMD	
3	VSS1	VDD1
4	VDD	
5	CLK	
6	VSS2	
7	DAT0	RCLKP
8	DAT1	RCLKM
9	DAT2	
10		VSS3
11		D0P
12		D0M
13		VSS4
14		VDD2
15		D1M
16		D1P
17		VSS5
CD	CARD DETECT	
WP	WRITE PROTECT	

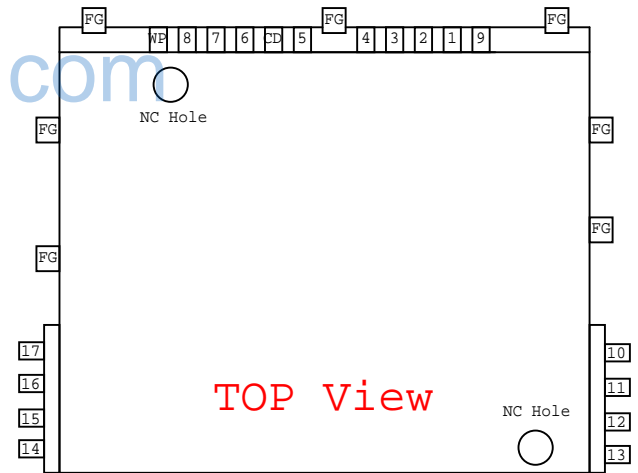
Bottom View



UHS II Interface	UHS I Interface
4 VDD1 3.3V	1 CD/DAT3
7 RCLKP	2 CMD
8 RCLKM	3 VSS1
10 VSS3	4 VDD 3.3V
11 D0P	5 CLK
12 D0M	6 VSS2
13 VSS4	7 DAT0
14 VDD2 1.8V	8 DAT1
15 D1M	9 DAT2
16 D1P	
17 VSS5	



CD : Low => Insertion Card  
High => No Card  
WP : Low => Write Protection On  
High => Write Protection Off or No Card



TOP View

UHS II slot

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**MEDIACARD SLOT**

Size  
A4

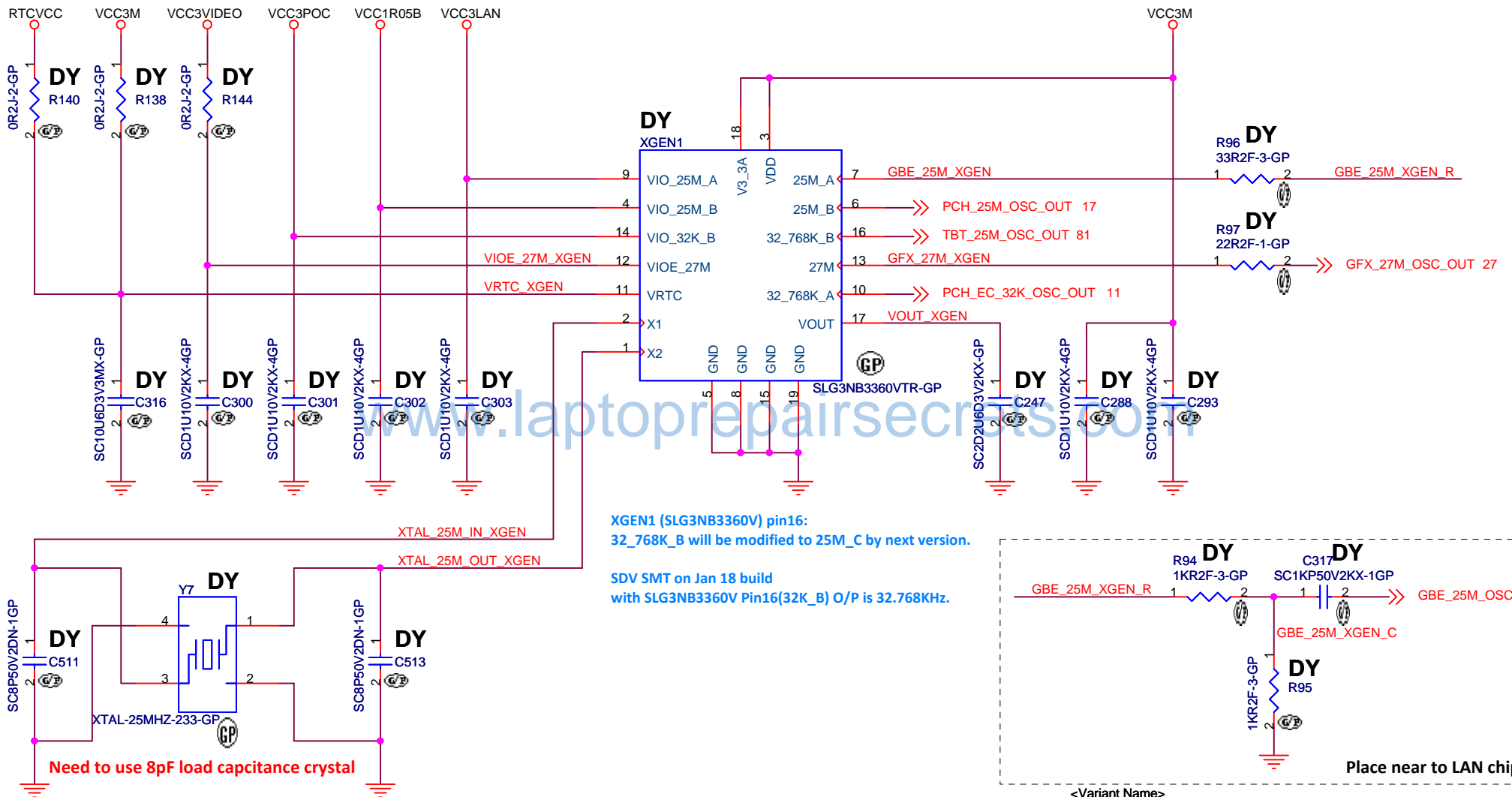
Document Number

**Kome-1 WS**

Rev  
-1

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Crystal 25MHz 10pF 30ppm			
KDS	DSX211G	1ZZCAA25000CC0C	82.30020.N91
TXC	8Y250	8Y25000010	82.30020.P11
EPSON	FA-128	Q22FA1280021400	82.30020.P61

**緯創資通**

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**CLOCKGEN**

Size A4

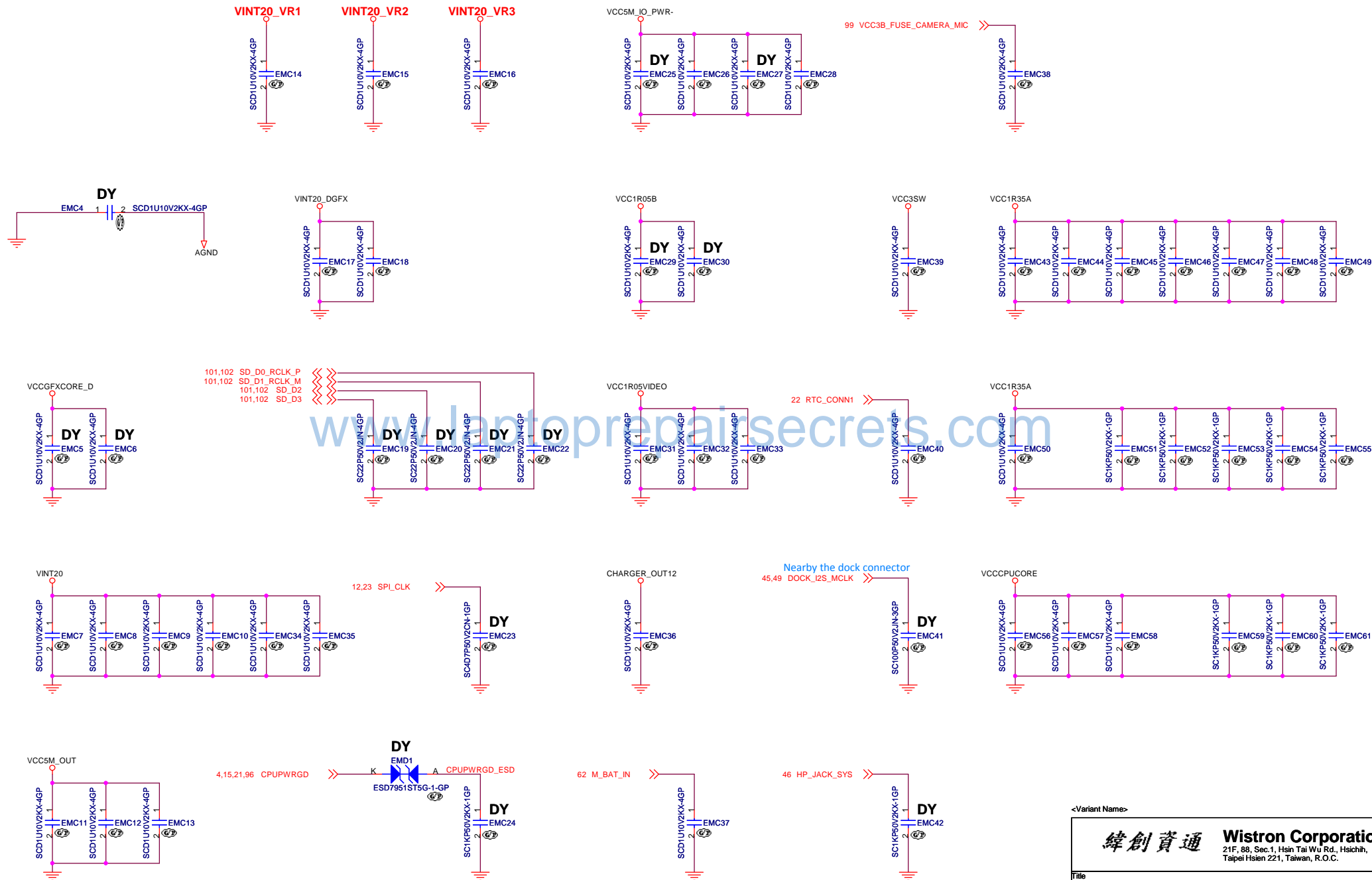
Document Number

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Date: Thursday, September 12, 2013

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Long power trace EMI decoupling caps





DOCK DP Switch		
Vendor	Vendor PN	Wistron PN
NXP	CBTL04083ABS	71.04083.003
Pericom	PI3PCIE3412ZHE+DAX	71.33412.B03

Change to NXP CBTL04083ABS as primary  
and drop TI because it uses Cu wire bonding.  
We should use Au wire bonding.

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